Poster Session 3

EDA & Testing

Date/Time	8/3(四)11:30—12:30
Chair(s)	李濬屹／國立清華大學資訊工程學系

PE01

VLSI Design of New Sorting Method Implements to the ORBGRAND

Szu-Hao Huang and Cheng-Hung Lin
Department of Electrical Engineering, Yuan Ze University

Guessing Random Additive Noise Decoding (GRAND) is a newly proposed error correction code that finds error patterns to correct the additive noise. Order Reliability Bits GRAND (ORBGRAND) used Log Likelihood Ratio (LLR) to generate error patterns to get a more probable pattern. In this paper, we proposed a new sorting method that can implement in the ORBGRAND. The proposed method is expected to reach low-cost and high-speed hardware of the ORBGRAND.

PE02

Layout Modification for Preventing Single-Event Double-Node Upsets in Latch Designs

Sam M.-H. Hsiao, Lowry P.-T. Wang, Charles H.-P. Wen
Institute of Electrical and Computer Engineering, National Yang Ming Chiao Tung University

Single-event-induced soft errors are serious issues in advanced nano-scale technology, causing malfunctions in systems. As the size of technology node decreases to sub-65nm with closer transistor spacing, single-event double-node upsets (SEDU) occur more frequently than single-event upsets (SEU).

In this paper, we propose a layout modification method to reconstruct the latch design, achieving 100% SEDU tolerance. Based on the concept of engineering change order (ECO), our layout modification method can prevent SEDU with minimum modification on layout. Experiments show that the reconstructed design can achieve a 100% soft error protection rate with the costs of an increment of 6.4% in area, 1% in timing and power penalty. The results indicate that our layout modification method can fully prevent SEDU by reconstructing the latch with minimum performance penalties.

PE05

A Hybrid CNN-LSTM Network for ECG Classification and Its Software-Hardware Co-Design Approach

Yu-Wei Chang, Yu-Ting Chen
Department of Information and Computer Engineering, Chung Yuan Christian University

This research is briefly presenting an implementation of software-hardware co-design of a hybrid CNN-LSTM Network for ECG classification. In our experiment, we transformed the weight of CNN into ternary type and exponential type. And after the transforming we change all the parameters of CNN into integer. In the LSTM model, we use circulant matrix to reduce the space usage of the weight. Then we combine two model into a hybrid model for better ability of both feature extraction and sequential data analyzing.

PE07

Small Sampling Overhead Error Mitigation for Quantum Circuits

Cheng-Yun Hsieh and James Chien-Mo Li
Graduate Institute of Electronics Engineering, National Taiwan University

In reality, quantum states are affected by errors in quantum devices. Noisy intermediate-scale quantum (NISQ) devices are existing quantum devices that exhibit error. NISQ devices have too few qubits and too high error rates, such that quantum error correction is not feasible. Error mitigation is a very promising technique for realizing useful applications for NISQ. Probabilistic error cancellation (PEC) is a promising error mitigation technique that reduces the error rate without auxiliary qubits. However, the sampling overhead of PEC grows fast with the number of PEC mitigated gates. Hence, we proposed a macro gate PEC (MGPEC) technique that aggregates multiple gates as a single macro gate to reduce the sampling overhead. Our result shows that MGPEC reduces the sampling overhead by 49\% on the QFT7 under the IBMQ noise model, which simulates real operation conditions of quantum circuits.

PE09

Reliability and Yield Enhancement Techniques for NAND Flash Memory with Fine-Grained Redundancies

Shyue-Kung Lu, Shi-Chun Tseng, and Xin Dung
National Taiwan University of Science and Technology

Built-in self-repair (BISR) has been considered as the most cost-effective solution for enhancing yield and reliability of NAND flash memories. Traditional BISR techniques use spare columns and blocks as the basic replacement elements and are categorized as the coarse-grained BISR techniques (CGBISR). However, the repair efficiency is low due to the large granularity of spares. To cure this dilemma, fine-grained built-in self-repair (FGBISR) techniques are proposed in this paper. We first derive repairable fault types (RFTs) for the widely used flash memory fault models. The RFTs include bit-, word-, page-, column-, and block-repairable faults such that faulty cells can be repaired at the fine-grained levels. The corresponding FGBISR architectures are also proposed. A simulator was developed for evaluating repair rate, yield, and hardware overhead. Experimental results show that the repair rate can be raised significantly with negligible hardware overhead.

PE10

Logic Locking of Threshold Logic Gates for Resisting SAT Attack

Yueh Cho[1], Ting-Yu Yeh[1], Yu-Shan Lin[1], Yung-Chih Chen[1] and Wang-Dauh Tseng[2]
[1] Dept. of Electrical Engineering, National Taiwan University of Science and Technology
[2] Computer Science and Engineering, Yuan Ze University

Logic locking is an IC/IP protection technique that can prevent IC/IP piracy, overproduction, and hardware Trojans. Recently, threshold logic re-attracted attention from researchers due to promising hardware realization and its applications in machine learning. Although several electronic design automation techniques for threshold logic have been proposed, there is still a lack of research on logic locking for threshold logic. Thus, in this work, we propose an integer linear programming (ILP)-based method for locking a threshold logic gate (TLG) to resist SAT attack, which is one of the most powerful attack techniques against logic locking. We present the characteristics that an encrypted TLG should have for resisting SAT attack, and formulate the problem of computing the encrypted function as an ILP problem. Since the ILP formulation is not scalable to large TLGs, we further propose a heuristic to improve efficiency. The experimental results show that the proposed method can successfully encrypt the TLGs having less than 8 inputs with acceptable execution time.

PE11

Key-based Hardware Obfuscation for RTL Loop Designs

Yi-Chen Chen and Shih-Hsu Huang
Department of Electronic Engineering Chung Yuan Christian University

RTL locking is a design technique that enhances hardware security by obfuscating the circuit semantics. Several methods for RTL locking have been proposed in previous literature. Intuitively, using these methods in combination should provide greater security compared to using any single method alone. However, in this paper, we use loop design as an example to illustrate that using these methods simultaneously may not improve security due to semantic conflicts. Based on this observation, we analyze the feasibility of different combinations of methods. For feasible method combinations, we further analyze their design overhead. Our research findings can serve as guidelines for RTL loop hardware obfuscation design.

PE12

Fault-Tolerant Winograd Convolution with Redundant Interpolation

Heng Hsu, Che Lin, and Tsung-Chu Huang
Department of Electronics Engineering, National Changhua University of Education

Most recent advances in artificial intelligence mainly focus on further acceleration, reliability and security in safety-critical ap-plications including 6G StarLink, and automotive. We find that Winograd Convolutions possess both potentialities on accelera-tion and fault tolerance theoretically. Therefore in this paper, we firstly take the single-fanout property of Winograd products to develop an effective and efficient single-interpolation error model. Secondly, we improve the state-of-the-art interpolation-point selection algorithm by taking into the arithmetic weights of inte-ger multipliers. And finally we propose some single-error detec-tion and correction methods using redundant-interpolation tech-niques. From both derivations and evaluations, the proposed redundant-interpolation Winograd convolutions not only possess a beautiful and concrete theoretical basis, but also an error cor-rection capability with only quite few area overhead.

PE14

A Fast Behavioral Model for ReRAM Crossbar Array to Support the Verification of In-ReRAM Computing Design

Shih-Han Chang, Ray-Hong Yen, and Chien-Nan Jimmy Liu
Inst. of Electronics, National Yang Ming Chiao Tung University

In recent years, In-memory computing (IMC) technology becomes a popular architecture to solve the bottleneck of data movement in AI edge designs. However, In-ReRAM computing (IRC) suffered from large device variation and numerous nonideal effects in hardware. If the peripheral circuits, such as SA and ADC are verified with large ReRAM crossbar array, it is almost infeasible to check the digital/analog integration by transistor-level simulations due to their high complexity. In this paper, an efficient approach is proposed to build accurate behavioral models for the verification of ReRAM crossbar array and the peripheral circuits in IMC designs. As shown in the experimental results, the behavioral model reduces the simulation time for overall IRC system from several minutes to seconds and still retain high accuracy to provide necessary error information for designers.

PE15

Interconnect Delay Approximation Method Considering Process Variation

Cheng-Yen Liu, Yu-Min Lee
National Yang Ming Chiao Tung University

Interconnect physical variation makes wire delay shift from the nominal value, the delay uncertainty may cause timing violation or make design performance degrade. The traditional method to capture delay variation is time-consuming while the circuit is large, and, hence, the timing analysis will be expensive. We propose a fast statistical method to capture the delay and slew variation induced by process variations, including physical dimension and gate output slew uncertainty, which reduces a lot of rumtime cost in timing analysis and design optimization.

PE16

A Machine Learning Framework to Predict DRC Violations

Ching-Chao Ku, Wei-Kai Cheng
Department of Information and Computer Engineering, Chung Yuan Christian University

At the early stage of physical design, predicting the design rule check (DRC) violation is essential to make the physical design more efficiency. Various factors affect the

accuracy of a DRC machine learning predictor, that is, an effective feature extraction makes the predictor more powerful. In this paper, we propose a machine learning DRC violation prediction using random forest. Experimental results show that using the features that have more close relation with routing can make the predictor more efficiently.

PE17

Multi-pin Net Substrate Routing Framework for Fine Pitch Ball Grid Array

Ming-Yen Chuang Yi-Yu Liu
Department of Computer Science and Information Engineering, National Taiwan University of Science and Technology

The packaging substrate is an essential carrier for integrated circuits (IC) and printed circuit boards (PCB). The quality of substrate routing is a critical factor for the efficiency and accuracy of signal connection in the substrate. However, most of the available automatic substrate routers only focus on the part of two-pin nets, substrate engineers still need to complete the routing for multi-pin nets manually. It is inefficient, time-consuming, and error-prone, especially for a large number of pins in the net, and even delays the time to market. In this paper, we proposed a three-stage framework for multi-pin net routing on fine pitch ball grid array package, including pin grouping, minimum spanning tree topology generation, and group topology connection. It accomplishes not only the connection from finger to bump ball but also the connections between bump balls and between bonding fingers. Experimental results from 6 industrial designs demonstrate that our framework completes multi-pin net routing with better routing results.

PE18

A Machine Learning Technique for Crosstalk Prediction

Yi-Ting Hsu, Wei-Kai Cheng
Department of Information and Computer Engineering, Chung Yuan Christian University

With the advance of circuit complexity, crosstalk issue becomes more and more important. The reason of crosstalk is because unwanted inductive and capacitive coupling occurs between closely spaced signal lines to interfere with each other. The noise and latency caused by crosstalk has become a significant problem with today's technology. However, it will be time-consuming to evaluate crosstalk problem after the whole physical design process. In this paper, we propose a machine learning method to evaluate crosstalk problem in the stage of placement.

PE19

A Novel Task Deployment Framework for Heterogenous Multicore Systems: An Aging-Aware Perspective

Ing-Chao Lin[1], Jie-Shih Wang[1], Zheng-Wei Chen[2], and Yu-Guang Chen[2]
[1] Dept. of Computer Science and Information Engineering, Nation Cheng Kung University
[2] Dept. of Electric Engineering Nation Central University

The aging effects on modern ICs may cause longer circuit delays and potential system failures over time, which rises threats on modern heterogeneous multicore systems that process real-time applications. To mitigate these aging effects, various aging tolerance strategies have been proposed. However, previous studies often neglect the different characteristics of big and little cores, and seldom to take critical tasks with the strict timing requirements present in real-time applications into consideration. Task-to-core mapping algorithms without carefully considering factors mentioned above may lead to sub-optimal solution and may result in early system failure. In this paper, we present an aging-aware task deployment framework for real-time systems. In our framework, we apply the concept of asymmetric aging which reserves healthy cores for critical tasks in the later life stage while non-reserved cores handle tasks in the early life stage. By using the lowest voltage that meets task deadlines, the proposed strategy mitigates accelerated aging effects caused by higher voltages. This approach increases the number of cores capable of meeting timing constraints in the later life stage, reducing the risk of system failures. Experimental results demonstrate that the proposed framework can improving system lifetime up to 1.17x.

Poster Session 4

Analog & RF / Digital & System

Date/Time	8/4(五) 10:30—11:30
Chair(s)	陳聿廣／國立中央大學電機工程學系

PA17

A Hysteresis-Current-Controlled Buck Converter with Current-Sensing and Phase-Locked-Loops Techniques

Po-Ju Chiu, Jiann-Jong Chen
Department of Electronic Engineering, National Taipei University of Technology

This paper proposed an improved-hysteresis-current-controlled buck converter with new-type current-sensing techniques. This controlled circuit used a hysteresis-current-controlled circuit to achieve fast transient response and a new type current sensing circuit which reduced the power consumption and increased the overall system efficiency. This converter was fabricated with TSMC 0.18μm 1P6M process. The chip area is 1.12×1.18mm2, with an input voltage range of 2.7V-3.9V, an output voltage range of 0.5V-2.5V, and a load current range of 50mA-500mA. It operates at a frequency of 1.25MHz, and has transient responses of 2.7us and 2.4us, with amplitudes of 18mV and 11mV, respectively. The maximum efficiency is 86.67%.

PA18

An Adaptive On-Time Buck Converter with Pseudo-DCR Current-Sensing and Phase-Frequency-Locked Techniques

Zi-Ping Zuo, Jiann-Jong Chen
Department of Electronic Engineering, National Taipei University of Technology

This paper presents an adaptive on-time buck converter with new current-sensing and phase-frequency-locked techniques. The proposed converter achieves a fast-transient response and a wide output voltage range. The proposed buck converter is fabricated with TSMC 0.18μm 1P6M CMOS technology, and the chip area is 1.14 mm×1.03 mm. The measured results show that the output voltage is 1.6V, the load current changes from 50mA to 500mA, and the transient response from 50mA to 500mA is 2.2s and 2.5s, respectively. When the load current is 300mA, the maximum power efficiency is 90.65%.

PA19

A Fast Transient Response DC-DC Buck Converter with Multiple Ramps PWM Control

Jing-Ting Lee, Jheng-Jyun Lian, Yi-Zhan Zhuang, and Po-Yu Kuo
Department of Electronic Engineering, National Yunlin University of Science and Technology

This paper proposed a multiple ramps generator circuit to enable a DC-DC buck converter achieve fast transient response and stable output voltage under rapid changing load. In this paper, firstly, a voltage sensing circuit is connected to the output. When the load change is detected, the slope of the sawtooth wave is changed by the capacitor charging and discharging characteristics of sawtooth oscillator. Then, the pulse-width modulation will vary according to the duty ratio. Hence, the feedback time, recovery time, and overshoot/undershoot voltage can be reduced. The proposed circuit is fabricated by 0.18μm CMOS process technology. The circuit is composed of a buck converter circuit, a voltage sensing circuit, a bandgap circuit, an error amplifier, a Type Ⅲ compensation circuit, a sawtooth generator, a pulse-width modulation circuit, a SR latch, and a dead time circuit. From the post layout simulation results, the input voltage of buck converter is 3.3V and the output voltage is 1.8V. The overshoot voltage is 14.7mV and undershoot voltage is 15mV. The recovery time are 5.5μs and 5.8μs, respectively.

PA20

A 300mV Cold Start-up Circuit Shared The Inductor with A Thermoelectric Energy Harvesting System

Xin-Hao Yu, Po-Wei Lin, Cheng-Yang Hsu, Sandeep Kumar Yadav, Zu-Jia Lo, Sheng-Yu Peng
Department of Electrical Engineering, National Taiwan University of Science and Technology

A cold start-up circuit for thermoelectric energy harvesting systems is presented in this paper. The proposed cold start-up circuit shares the energy harvesting inductor and load capacitor with the main boost converter, so no extra off-chip components are required, resulting in a small form factor. The start-up circuit comprises a stacked ring oscillator, a pair of low-voltage charge pumps, a low-power voltage detector, a reset switch, and two power switches. A prototyped chip for concept proving is designed and fabricated in a 0.18 um CMOS process. The measured waveforms demonstrate that the prototyped cold start-up chip can boost an input voltage of 300mV up to 1V within 950ms when the loading capacitance is 0.1 uF.

PA21

A Low Output Voltage Ripple Buck Converter with Light Load Efficiency Improvement Using a Body-Controlled Zero-Current Detector

Chia-Ying Lee[1], Yuh-Shyan Hwang[1], Dong-Shiuh Wu[2]
[1] Department of Electronic Engineering, National Taipei University of Technology
[2] Department of Electronic Engineering, Lunghwa University of Science and Technology

A Low Output Voltage Ripple Buck Converter with Light Load Efficiency Improvement Using a Body-Controlled Zero-Current Detector(ZCD) designed and implemented using the TSMC 0.18μm 1P6M process. The voltage-squared ripple control mode is adopted in this buck converter. In the traditional ripple control buck converter architecture, the detected inductor current and output voltage ripple are superimposed as feedback signals to ensure stability even when there is low output voltage ripple, thereby improving the limitations of the traditional architecture when applied to loads with low ripple requirements. Additionally, a body-controlled ZCD is used to create an offset voltage on the comparator to counteract the delay of the comparator itself, logic, and driver, and to improve light load efficiency through precise ZCD. The chip area is 1.19979mm×0.888mm, the input voltage range is 2.8V-3.3V, the output voltage range is 1.2V-2.0V, and the load current range is 50-500 milliamperes. When the output voltage is 1.5V, the transient response of switching the load current from 50 mA to 500 mA and from 500 mA to 50 mA is 5.2 μs and 5.09 μs, respectively. At a load current of 300 milliamperes, the highest efficiency is 95.78%

PA22

An Adaptive On-Time Controlled Buck Converter with New-Rds,on-Current-Sensing Techniques

Yu-Zhih Zheng[1], Yuh-Shyan Hwang[1], Dong-Shiuh Wu[2]
[1] Department of Electronic Engineering, National Taipei University of Technology
[2] Department of Electronic Engineering, Lunghwa University of Science and Technology

This paper introduces a new type of buck converter that utilizes new techniques for Rds,on current sensing. The proposed converter can achieve high efficiency and fast transient response times. The converter is fabricated with TSMC 0.18μm 1P6M process, and the chip area is 1.2 mm×1.19 mm. The output load current range is 50~500mA. The load transient response times are about 2.34 μs and 2.13 μs when the load currents are light to heavy and heavy to light, respectively. The maximum peak efficiency is 93.58% when the output voltage is 1.2V and the load current is 300mA.

PA23

A V^2 Adaptive On-Time Buck Converter with Transient Accelerated Circuits

Yi-Pu Chen[1], Yuh-Shyan Hwang[1], Dong-Shiuh Wu[2]
[1] Department of Electronic Engineering, National Taipei University of Technology
[2] Department of Electronic Engineering, Lunghwa University of Science and Technology

This paper proposed A V2 Adaptive On-Time (AOT)Buck Converter with Transient Accelerated Circuits，AOT Control captures input and output information to adjust the conduction period of the circuit, generating a more stable operating frequency. Transient Accelerated Circuits adjust the on-time during current load switching in the circuit, allowing the transient voltage to return to a stable state in the shortest possible time. The proposed buck converter is fabricated in TSMC 0.18um 1P6M CMOS processes with a chip area of 1.19mm × 1.088mm. The measurement results show that the transient recovery times are 1.3μs and 1.4μs, and the undershoot and overshoot voltages are 9mV and 15.3mV, when the load current changes from 50mA to 500mA and from 500mA to 50mA. The peak power efficiency is 93.86%, when the load current is 300mA and output voltage is 1.8V.

PA24

Digital IC & DSP Controller Design for Boost Converter Base on SIMPLIS-VH/SIMetrix

Yuan-Dong Huang, Wei-Ting Yeh, Chun-Yen Chen, Jen-Chieh Cheng and Chien-Hung Tsai
Department of Electrical Engineering National Cheng Kung University

In the field of power systems, initial system design is often completed using MATLAB, Simulink, PLECS, SIMPLIS & SIMetrix, while later chip design is carried out using relevant software provided by Cadence or Synopsys. However, this approach requires switching the system to different design platforms for simulation and verification, which takes additional time to rebuild the system. Therefore, this paper proposes a new design process to implement a digital boost converter using SIMPLIS & SIMetrix for both system and chip design, enabling design and verification to be completed on a single platform without the need to change the simulation platform and save time on rebuilding the system. The digital controller in this paper is implemented using TSMC 0.18um CMOS process and compared with the traditional design process using Cadence.

PD19

Rapid and High-Sensitive Admittance Sensor for Sweat Analysis

Jia-Yo Chang, Ji-Zun Chen, Han-Hsiang Chu, Yan-Xin Chen, Chun-Chi Chen
Department of Electrical Engineering, National Chiayi University

Sweat analysis has emerged as a promising approach for detecting various diseases and monitoring health conditions.

In comparison to conventional blood tests, sweat analysis offers the advantage of non-invasiveness and low infectious risk.In this study, we have developed a sensitive and reusable electrolyte analysis device.The device utilizes electrode plates to measure the corresponding admittance of the test sample, and then amplifies the subtle signal response for observation. The designed sensor device can be applied to estimate the ion concentration of electrolytes in sweat with high sensitivity and stability, thereby enabling the detection of changes in individuals' health status.The affordability and reusability of this rapid sweat analyzing system make sweat a valuable and reliable health indicator, in line with the principles of low-cost and accessible healthcare technologies.

PD20

Design and Implementation of a Plant Electrophysiological Signal Identification Method Based on LSTM Convolutional Networks

Yang-Chi Chen[1] and Chi-Chia Sun[1,2]
[1] Department of Electrical Engineering, National Formosa University
[2] Smart Machine and Intelligent Manufacturing Research Center, National Formosa University

With an increasing number of practical applications, research on plant sensing has been receiving constant attention. The aim of the research is not to simply demonstrate that "plants have thoughts", but to explore why and how plants perceive their surrounding environment. Both animals and plants have been using signals that contain specific chemical substances to communicate with the outside world. Plants, for example, use chemical substances to communicate, grow, and defend themselves.

We have developed a new electrophysiological sensor that serves as an autonomous device to demonstrate plant thinking, which can transmit plant potential data transformed into plant autonomous consciousness signals. Plant sensing can measure certain aspects of the natural plant's internal state, and the sensor circuit design is based on electrophysiological methods used in electrocardiography and electroencephalography. We use plant electrophysiological methods to collect physiological data and perform data analysis to infer the plant's behavior. Among many neural networks, we have chosen the LSTM (Long Short-Term Memory) neural network

for analysis. The LSTM neurons retain memory context in their pipelines, allowing them to address sequencing and time issues without suffering from gradient vanishing problems that can affect performance. They can solve the continuous changes in physiological timing correlations in plants.

Index terms: plant sensing, plant electrophysiology, neural networks.

PD21

Distributed IoT Access Control Mechanism with Ureka

Yi-Hung Huang[1], Yi-Chun Yang[2], Ren-Song Tsay[2], 4Wei-Chung Chen[3]
[1] Department of Electrical Engineering, National Tsing Hua University
[2] Department of Computer Science, National Tsing Hua University
[3] Institute of Information Systems and Applications, National Tsing Hua University

The rapid expansion of IoT technology has resulted in significant productivity and efficiency gains for individuals and organizations. Nevertheless, current centralized access control systems present significant security and privacy risks. To address these concerns, this paper proposes a distributed self-sovereign access control mechanism for IoT that supports secure authentication and authorization with clear accountability. We present a complete solution for managing ownership in IoT, including establishing and transferring ownership. Our cryptography-based approach, utilizing the "U-ticket" and "mini-firewall," enables a secure and efficient exchange of access control messages among owners, users, and devices, resulting in a robust IoT ecosystem. Our design grants self-sovereignty to device owners, enabling them to manage their devices independently, reducing device costs, and increasing security by eliminating the need for Internet connectivity. This paper demonstrates how the U-ticket and mini-firewall method provides a comprehensive solution for device initialization, ownership management, authorization, revocation, and identity verification, while maintaining security and privacy in the IoT system.

PD22

Automated Classification of Multi-class Eye Disease with Lightweight CNN Architecture and Weighted Volume Test

Min-Chun Hou[1], Cheng-Hung Lin[1,2], Cheng-Kai Lu[3], Jia-Kang Wang[1,4], Tzu-Lun Huang[1,4]
[1] Department of Electrical Engineering, Yuan Ze University
[2] Biomedical Engineering Research Center, Yuan Ze University
[3] Department of Electrical Engineering, National Taiwan Normal University
[4] Department of Ophthalmology, Far Eastern Memorial Hospital

As deep learning development becomes more mature, there are a lot of models are developed toward deeper. However, we think that 3D-optical coherence tomography (OCT) eye image classification may not need a complicated model. And also, there exists a study that confirms our speculation. Therefore, we are trying to employ the simpler convolutional neural network (CNN) model on multiple eye disease classification. One is the lightweight model MobileOCT and it reaches an accuracy of 87.03%. The other is the proposed Lighten Modified A-OCT achieving an accuracy of 89.82%. Besides, we also proposed the weighted volume test to solve the problems that will meet in the realistic case.

PD23

Optimizing Real-time Bearing Remaining Useful Life Prediction through Health Stage and Dynamic Feature Selection Division based on Monotonicity

Kun-Chih (Jimmy) Chen[1], Zhe-Xiang (Sean) Tu[2] and Chen-Jyun (Justin) Tang[2]
[1] Institute of Electronics, National Yang Ming Chiao Tung University
[2] Department of Computer Science and Engineering, National Sun Yat-sen University

Rotating machinery is widely used in various fields, such as wind turbines, car engines, and various machines in factories. It is evident that the maintenance strategy for rotating machinery is crucial. Therefore, predicting the remaining useful life (RUL) of machinery is beneficial in formulating suitable maintenance strategies and reducing maintenance costs. Due to unpredictable human errors and uncontrollable factors during operation, it is difficult to evaluate the RUL of machinery using simple methods. Traditional RUL prediction methods also cannot adjust the prediction model in real-time with the current status of the machinery or factory. We propose an RUL prediction method based on an artificial neural network (ANN) and an adjustment technique using root mean square (RMS) to simplify computations and improve real-time results. Finally, compared to related research methods, we were able to dynamically adjust appropriate features based on the machinery state, resulting in a reduction of errors by 95.59% to 97.76% and a decrease in the number of parameters by 96.92% to 99.36%, achieving lower computational costs.

PD24

Distributed Self-Sovereign IoT Access Control Transaction Management

Young Ya[1], Yi-Chun Yang[2], Ren-Song Tsay[2], Wei-Chung Chen[3]
[1] Department of Electrical Engineering, National Tsing Hua University
[2] Department of Computer Science, National Tsing Hua University
[3] Institute of Information Systems and Applications, National Tsing Hua University

This paper proposes a user-centric solution for transaction management in the Internet of Things (IoT) by integrating blockchain smart contract technology with the Ureka IoT architecture. Traditional IoT provider-centric management systems face significant security, privacy, and dispute resolution challenges, making a shift towards self-sovereign access management systems necessary. The proposed design empowers IoT device owners and users to manage access controls and transaction data while maintaining privacy, security, and trust. One significant advantage of the proposed design is that IoT devices do not require an internet connection, reducing device costs and energy consumption. Users can use a mobile device as an intermediary for secure and trustworthy access to the target device. The proposed solution offers flexible device deployment locations, reduced device costs and energy consumption, and secure self-sovereign IoT infrastructures.

PD25

An Automatic Detection System of Multiple Eye Diseases Based on Extreme Learning Machine

Wei-Chen Kuo[1], Cheng-Hung Lin[1,2], Cheng-Kai Lu[3], Jia-Kang Wang[1,4], Tzu-Lun Huang[1,4]
[1] Department of Electrical Engineering, Yuan Ze University
[2] Biomedical Engineering Research Center, Yuan Ze University
[3] Department of Electrical Engineering, National Taiwan Normal University
[4] Department of Ophthalmology, Far Eastern Memorial Hospital

In recent years, machine learning (ML) has been combined with more and more research in the field of medicine. This research hopes to use ML to assist ophthalmologists in diagnosing eye diseases. Optical coherence tomography (OCT) images provide high-resolution images of the eyeball. Therefore, this paper attempts to use OCT images combined with ML to build an automatic detection system for eye diseases. This research uses extreme learning machine (ELM) as an ML classifier, and takes advantage of its high-speed operation and easy hardware implementation to achieve the goal. Although the current accuracy can only reach 69.09%, the prototype of the automatic eye disease detection system has been successfully built, and it is hoped that the process can be improved in the future to achieve high accuracy.