# Poster Session 1

## Analog & RF

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| Date/Time | 8/2(三)13:30—15:00 |
| Chair(s) | 蔡政翰／國立師範大學電機工程學系 |

PA01

### Chip Design of High-Speed LIDAR Driver

*Shih-Chang Hsia ,and Tse-Fu Chang*
*National Yunlin University of Science and Technology*

LIDAR (Light Detection and Ranging) technology is commonly used in vehicles to detect obstacles and enable advanced driver assistance systems (ADAS). The driving chip designed in this paper is specifically designed to provide high-speed transmission for LIDAR systems. The chip utilizes a multiple phase method for the charging and discharging sequence of three power MOSFETs, resulting in reduced rise and fall times of the current pulse, and ultimately achieving a high and fast driving circuit. The chip was manufactured using TSMC 0.18μm CMOS HIGH VOLTAGE MIXED SIGNAL process technology. The measured results of the chip show that the pulse rise time and fall time are only 3.08ns and 4.09ns, respectively, with a driving current of 1.14A. This indicates that the chip can provide high-speed transmission for LIDAR systems, enabling them to detect obstacles quickly and accurately.

PA02

### A Silicon-based Data Isolator for Signal Transmitter

*Shih-Chang Hsia, Yuan Heng Wang and Hung-Lieh Chen*
*National Yunlin University of Science and Technology*

This study presents an isolated signal transmission with a silicon chip. The transmission media uses RF signal rather than optical signal. The function of this chip likes the conventional optical coupler that is applied to isolate the input and output for power supply system. The feedback control signal is modulated with RF signal and then it can pass a snake line for data transmission. The advantages are that the data transfer rate is higher than the conventional optical coupler. Besides, the implementation cost is cheap and it can be easily integrated to the current CMOS chip. This chip is designed with full-costumed methodology. The chip area included pads is only 1.5mm2 using TSMC 0.25m high-voltage technology.

PA03

## The Design and Implementation of A Reconfigurable Filter Using Floating-gate Transistors and Capacitors

*Chun-Jui Chen, Bipasha Nath, Hung-Yu Shih, Sheng-Yu Peng*
*National Taiwan University of Science and Technology*

This paper presents a fully reconfigurable floating-gate-transistor-capacitor (FGT-C) filter that is compact and power efficient. The proposed filter employs a compact biquadratic section, which provides both lowpass (LP) and bandpass(BP) outputs with programmable filter parameters, including the gains, natural frequency, quality factor, and DC levels for input and output signals. In addition, the topology of the FGT-C filter exhibits modularity. The biquadratic sections can be cascaded and scaled up easily to implement high-order frequency responses. A prototyped chip has been fabricated in a 0.35μm CMOS process, with each biquadratic section occupying an area of 0.0313mm2 . The measurement results were taken with a supply voltage of 1.8V and both output voltage level programmed at 0.9V . From measurements, the biquadratic FGT-C filter consumes 118.4nW of power with a spurious free dynamic range of 43dB in a 10kHz bandwidth setting. It is suitable for low-power analog signal processing in large-scale field programmable analog arrays.

PA04

## The Back-end Circuit to Calibrate the Hysteresis and Drift Effect of the RuO2 Dopamine Biosensor

*Ming-Tai Hsu[1], Po-Yu Kuo[1],*, Jung-Chuan Chou[1], Po-Hui Yang[1], Chih-Hsien Lai[1], Yu-Hsun Nien[2], Tai-Hui Wang[1], Che-Tsung Chan[1], Ying-Sheng Zhang[1], Chi-Han Liao[1], Wei-Shun Chen[1], Jun-Ming Huang[1], Hao-Jun Hu[1]*
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In this study, we proposed a new method to address the issue of hysteresis and drift effect in ruthenium dioxide (RuO2) dopamine biosensors. Specifically, we designed and implemented a back-end calibration circuit that was able to significantly reduce both hysteresis and drift effects in the biosensors. To test the effectiveness of the proposed method, we first fabricated a RuO2 dopamine biosensor and measured its drift rate and hysteresis voltage using a voltage-time measurement system. The back-end calibration circuit is applied to calibrate the drift and hysteresis of the sensor. The results showed that the proposed back-end calibration circuit was able to reduce the drift rate by 99.62% and the hysteresis voltage under forward cycle and reverse cycle by 86.02% and 85.98%. Therefore, the proposed approach is successful and practical in tackling the problems of hysteresis and drift effect in RuO2 dopamine biosensors.

PA05

## Design and Implementation of a Glucose Sensor Integrated with Readout Circuit: Sensing Characteristics and Validation

*Chi-Han Liao[1], Po-Yu Kuo[1]*, Jung-Chuan Chou[1], Po-Hui Yang[1], Chih-Hsien Lai[1], Yu-Hsun Nien[2], Tai-Hui Wang[1], Che-Tsung Chan[1], Ying-Sheng Zhang[1], Ming-Tai Hsu[1], Wei-Shun Chen[1], Jun-Ming Huang[1], and Hao-Jun Hu[1]*
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This study presents the design and implementation of a glucose sensor integrated with a self-designed readout circuit. The glucose sensor utilizes a GOx/RuO2 biosensing mechanism, while the instrumentation amplifier incorporates a two-stage CMOS op-amp. The fabrication process involves the deposition of GOx/RuO2 thin films using an radio frequency (R.F) sputtering system on a flexible printed circuit board. The fabricated biosensors are stored at low temperature. The proposed readout circuit consists of a voltage-feedback instrumentation amplifier (VFIA) and a programmable gain amplifier (PGA). This circuit exhibits programmable gain control through the replacement of resistor with transmission gates and a decoder. Post-layout simulations are conducted to validate the designs. From the results, the Gox/RuO2 glucose biosensors showed a sensitivity and linearity of 50.21 mV/mM and 0.997, respectively. These findings highlight the potential of the integrated glucose sensor and instrumentation amplifier for accurate glucose measurement in healthcare applications.

PA06

## A Continuous Time Delta-Sigma ADC with VCO-Based Quantizer

*Tsai-Feng Wu, Man-Chen Huang, Jie-Syuan Lin, Jhe-Wei Li, Zhen-Jie Hong*
*Department of Electronic Engineering, Feng Chia University*

This paper proposed a VCO-based integrator and quantizer within a continuous-time (CT) delta-sigma analog to digital converter (DSADC) for ultrasound testing over a 10 MHz signal bandwidth with a 1GHz sampling rate and the oversampling rate to be 50 times. The prototype ADC achieves a 61 dB signal-to-noise ratio (SNR), and 9.8bits effective number of bits (ENOB), respectively, over a 10 MHz signal bandwidth with a 1 GHz sampling rate. The whole ADC total consumes 43.9 mW of power from a 1.8 V power supply in a TSMC 0.18μm CMOS process.

PA07

## An 8-bit 10-MS/s Weight-merged SAR ADC for Real Time Illness Detecting System

*Yu-Wei Chang, Ming-Yueh Ku, Hao-Yun Lee, and Shuenn-Yuh Lee*
*Department of Electrical Engineering, National Cheng-Kung University*

This paper presents a successive approximation registers analog-to-digital converter (SAR ADC) combined with the binary weighting operation of multiplication and accumulation (MAC) of computing in memory (CIM). This proposed architecture can not only save the power consumption from digital circuits and data converters but improve the area efficiency of the circuit by reusing the capacitor array of SAR ADC, making this architecture more beneficial for the low power design on a system overview. Simulation results show that this proposed ADC operating at 10 MS/s can achieve a signal-to-noise and distortion ratio (SNDR) of 49.91 dB while consuming 192.13 μW under 1.2 V supply voltage, which achieves the high energy-efficiency and accuracy for the edge illness detecting applications.

PA08

## Third-Order One-Bit Switched-Capacitor Delta-Sigma Modulator with a Cascaded Integrator Feedforward Topology

*Guo-Ming Sung, Sian-Wei Chao, Yan-Fan Jiang, Li-Ling Zhou, and Chih-Ping Yu*
*Department of Electrical Engineering, National Taipei University of Technology*

This paper proposes a third-order switched-capacitor (SC) delta-sigma modulator (DSM) with a cascaded integrator with feedforward (CIFF) architecture. The destination is not only to eliminate the non-ideal effects in capacitor array but also to improve the performance of the integrator. The Simulink software is used to determine those important coefficients and to guarantee the stability and functionality of the proposed three-order delta-sigma modulator. The proposed SC DSM will be designed and verified based on the UMC 0.18-m CMOS process. The gate-level simulation results show that the signal to noise-and-distortion ratio (SNDR) is approximately 105.9 dB and the power consumption of 5.0 mW at the bandwidth of 20 kHz, sampling frequency of 2.5 MHz, and over-sampling ration of 128.

PA09

## A Voltage to Digital Converter for RC Coefficient Calibration in CTDSM with Self-Calibrating Low-Offset Comparator

*Yin-Qin Ye[1], Sheng-Shiang Lai[1], Chuang-Hsuan Chueh[1], Hsin-Liang Chen[2], Jen-Shiun Chiang[1]**
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This paper presents a 9-bit voltage to digital converter (VDC) that converts DC voltage into digital codes. The VDC utilizes a counting-based approach and includes a self-calibrating comparator. The comparator performs calibration by controlling the number of compensating MOS transistors connected to the main input pair. Through Monte Carlo simulations, the self-calibration reduces the standard deviation of the offset ($\sigma$os) of the comparator from 4.27 mV to 0.527 mV at a speed of 50 MHz. Furthermore, it ensures that the VDC avoids digital code conversion errors caused by MOS mismatch in the comparator. The linearity of the VDC, evaluated by linear regression with an R-squared value, reaches 0.9999 at a conversion period of 16 μs.

PA10

## High resolution TDC implementation on cyclone V FPGA

*Cheng-Sheng Lin, Yu-Cheng Cai, and Chun-Chi Chen*
*Department of Electrical Engineering, National Chiayi University*

Numerous research papers have proposed the use of Tapped Delay Line (TDL) based Time to Digital Converters (TDCs) on Field-Programmable Gate Array (FPGA) targets. However, these works often neglect to address the timing challenges that arise due to routing delays. This study aims to draw attention to the key timing considerations that must be taken into account when implementing TDCs in FPGA targets and suggest practical solutions to address these issues. The paper also includes a detailed design methodology for a TDC on a Cyclone V FPGA target as a case study

PA12

## A 27-31 GHz 7-bit Vector-Sum Phase Shifter For LEO Satellite Communication Transmitter

*Hao-Jen Tu, Hsiao-Chin Chen*
*Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology*

This paper presents a 7-bit digital control vector sum phase shifter for LEO satellite communications. The circuit consists of a quadrature all-pass filter (QAF) and an analog

differential adder that is biased with an 8-bit current digital-to-analog converter (IDAC), where the IDAC is used to control the bias current of the analog adder so that the phase shit from 0 to 360 degree can be generated in steps of 2.8 degree. Consuming the power of 10 mW and die area of 0.7 mm2, the phase shifter achieves a RMS phase error of < 0.66 degree and a RMS amplitude error of < 1.5 dB.

Index Terms—Active phase shifters, vector sum phase shifter, current DAC, digital control, phased arrays, LEO Satellite Communications.

PA13

### A W-Band SSB Up-Conversion Mixer in 90-nm CMOS

*Yen-Chung Chiang, Hao-Yu Lin and Yu-Ru Lin*
*Department of Electrical Engineering, National Chung Hsing University*

In this paper, a single-sideband (SSB) up-conversion mixer implemented in the TSMC 90-nm CMOS process technology for W-band applications is presented. The quadrature signals for local oscillation (LO) signals and I/Q baseband signals are generated by Lange couplers and polyphase filters, respectively. The measured conversion gain of this fabricated chip is –4.17dB under a LO power of –2dBm. To validate the feature of the single sideband mixer: the measured image rejection and LO leakage suppression are –25.94 dBc and –32.98 dBc, respectively. The chip area of the proposed mixer is 0.932×0.603 mm2, and the power consumption is 16.75 mW at a 1.2-V supply voltage.

PA14

### A 7-bit K-Band Vector-Sum Phase Shifter for LEO Satellite Communication Receiver

*Pin-Shuan Chen and Hsiao-Chin Chen*
*National Taiwan University of Science and Technology*

This paper presents an active type 7-bit vector-sum phase shifter (VSPS) for K-band (17-21 GHz) low earth orbit satellite communication, implemented and fabricated in a TSMC 90-nm CMOS technology. The phase shifter employees a resonance-based quadrature all-pass filter and an analog vector adder that is biased with 8-bit current digital-to-analog converters (IDACs). According to simulation results, the phase shifter achieves the RMS phase error of 0.23~0.75 and the RMS amplitude error of 1.05 ~ 1.9 dB. The core chip size is 0.76 (mm)^2. The phase shifter dissipates the total power consumption of 8.04 mW from the 1.2 V supply voltage.

PA15

## A Wide Range Digital To Time Converter used Phase Compensated Fractional Divider in 180-nm CMOS

*Jiang Zheng, and Ching-Yuan Yang*
*Department of Electrical Engineering, National Chung Hsing University*

A fractional divider using delta sigma modulation (DSM) with 10-bit digital to time converter (DTC) to achieve true division of fractional,the proposed DTC based on the delay lock loop (DLL) phase compensation calibration to make the DTC phase error compensation more suitable for high resolution.With the basis of Fractional-N divider technology,we can improved noise problem in fraction spur.

The proposed fractional divider is operation range from 0.4G to 2.4G,when input frequcency is 0.4G,the peak to peak jitter is reduced from 2.5ns to 80ps after compensation, when input frequcency is 2.4G,the peak to peak jitter is reduced from 415ps to 25ps after compensation.

PA16

## Low Power Low Noise Receiver With Sub-Harmonic and Gain Enhanced N-Path Mixers

*Yi-Hsuan Hsia, Ming-Hsuan Kuo, and Kuang-Wei Cheng*
*National Cheng Kung University*

This article presents a low-power and low-noise dual-conversion receiver with power-saving and gain-enhancing mixer technologies. In the RF front end, the LNA is currently reused with a 4x sub-harmonic mixer, so the LO frequency is internally multiplied, thus reducing the power burden of the local oscillator. In the low second-IF conversion, an N-path mixer is implemented together with a frequency-shift bandpass filter for the channel selection. Designed in 90-nm CMOS technology, the receiver can achieve a noise figure of 6.6 dB, and a conversion gain of 80 dB with a power consumption of 151 μW.