Oral S20

Emerging Testing and Physical Design

Date/Time	8/4(五) 10:30—11:30
Chair(s)	温宏斌／國立陽明交通大學電機工程學系 陳勇志／國立臺灣科技大學電機工程學系

S20.1 | 10:30—10:45

Test Compression for Neuromorphic Chips

Xin-Ping Chen[1], Hsu-Yu Huang[1], Jennifer Shueh-Inn Hu[2], and James Chien-Mo Li[1]
[1] National Taiwan University; [2] Ming Chuan University

We propose test compression techniques to reduce the test time (test configurations and test length) for neuromorphic chips. Our test compression techniques include Dynamic Test Compression (DTC) and Static Test Compression (STC). DTC generates test configurations with machine learning. STC reduces test length under the constraint of the significance level in Two-sample Hotelling's T-square test. Experiments on two neuromorphic architectures show that our proposed techniques can reduce the total test configurations by 90.44% and the total test length by 93.64%, respectively. Our run time is more than 10x faster than the previous method. The proposed techniques are independent of neuromorphic chips' applications.

S20.2 | 10:45—11:00

Diagnosis of Systematic Delay Failures through Subset Relationship Analysis

Bing-Han Hsieh[1], Yun-Sheng Liu[1], James Chien-Mo Li[1], Chris Nigh[2], Mason Chern[3]
[1] Graduate Institute of Electronics Engineering, National Taiwan University
[2] Qualcomm Technologies, Inc.
[3] Qualcomm Semiconductor Limited

Delay faults have become increasingly important in modern designs due to decreasing technology node size and increasing operation frequency. However, diagnosis of delay faults can be challenging since there are typically few of failing bits in the test failures. In this work, a two-phase flow is presented to identify systematic delay failures and improve their corresponding diagnosis resolution. First, the subset relationships among test failures are analyzed to identify systematic defects. Then, representative test failures in the subset relationships are selected for diagnosis of the defect behavior. Experiments on two cores of an industrial design with three cases show over 33x, 69x,

and 8x improvement on delay fault diagnosis resolution. Furthermore, the proposed technique can be easily integrated with commercial tools.

S20.3 | 11:00—11:15

Multi-Row Guiding Template Design and Layout Optimization for Lamellar DSA with Self-Aligned Via Process

Yi-Ting Lin, Kang-Ting Fan, and Iris Hui-Ru Jiang
Graduate Institute of Electronics Engineering, National Taiwan University

Directed self-assembly (DSA) of block copolymers (BCPs) can generate tiny and dense layout features, holding great potential for patterning vias/contacts at advanced nodes. Existing studies mainly focused on guiding template design for cylindrical DSA, but by leveraging selfaligned via (SAV) process, lamellar DSA can form vias to be immune to placement errors and free of a uniform pitch between vias, which cylindrical DSA suffers from. The state-of-the-art guiding template design for lamellar DSA can handle only single-row templates, thus limiting the flexibility of via grouping. Therefore, in this paper, we explore further and propose a novel and general multi-row guiding template design approach. We also devise a post-routing layout optimization scheme to make the layout more friendly to this process. Experimental results show that our approach outperforms the state-of-the-art work on both mask conflicts and short guiding templates, and requires much less computation time. On the other hand, the proposed layout optimization scheme can further improve the via manufacturability.

S20.4 | 11:15—11:30

Routing demand Prediction With Extreme Gradient Boosting (XGBoost)

Shih-Cheng Huang[1], Yu-Guang Chang[1], Cheng-Hong Tsai[2], De-Shiun Fu[2], Mango Chia-Tso Chao[3]
[1]National Central University; [2]Global Unichip Corporation; [3]National Yang Ming Chiao Tung University

The routing stage in Very Large Scale Integrated Circuits (VLSI) physical design flow is one of the most time-consuming stages. With the increasing complexity of designs, this stage often requires several days of effort to find a routing solution without design rule violations (DRV). However, a design with inadequate routing resource results in routing congestion and DRV. Moreover, the situation that with insufficient routing resource is influenced by previous stage, so that engineers have to adjust design in previous stage and routing again. According that routability estimation is important to avoid unnecessary routing when routability is unacceptable. In this paper, we proposed an approach based on ensemble learning to predict global routing demand in the placement stages, aim to reduce the number of iterations in the physical design

procedure. We quantify placement information into grid-based features and built XGBoost model to predict global route results. Experiment result show that our model achieves Pearson Correlation Coefficient (PCC) of 0.918 and R-squared of 0.834 in routing demand prediction. Furthermore, our method achieves average speed up of x 0.008 compare to commercial global router. In summary, our method saves time and effort that reduce the need for execute routing repetitively.