Oral S19

Circuits and Systems for BioMedical/BioSignal Applications

Date/Time	8/4(五)　10:30—11:30
Chair(s)	湯松年／中原大學資訊工程學系 龔存雄／長庚大學電機工程學系

S19.1 | 10:30—10:45

Design and Implementation of Bio-Signal Processor for Wearable Device Applications

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Wearable devices can constantly monitor human bio-signals and help maintain and even improve human health conditions. One of the key components in a wearable device is a bio-signal processor capable of realizing low-power computations. We demonstrate that both processor performance and efficiency could be significantly enhanced by utilizing efficient processing algorithms and hardware architecture. A design of a bio-signal processor is presented as an implementation example for low-power wearable device applications.

S19.2 | 10:45—11:00

Portable and High Accuracy EIS System Design with a Low-Complexity Impedance Calculation

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This paper presents a novel low-complexity impedance calculation based on a compact recursive discrete Fourier transform (RDFT) for electrical impedance spectroscopy (EIS) system design. Compared to a traditional fast Fourier transform, an arbitrary-length RDFT is not limited by the powerof-two transform length. By choosing a suitable integer ratio of the desired frequency/frequency resolution, the spectrum leakage can be

significantly reduced by 4-Hz resolution per bin, which enables a lower magnitude relative error (MRE) and a phase absolute error (PAE) in impedance calculations. Here, the practical measurement results show that the maximum MRE and PAE are below 0.1% and 0.5°, respectively, making this approach superior to previously reported ones. Compared with the state-of-the-art Goertzel filter-based EIS system, the proposed method provides more frequency bins (+43.75%) within the same frequency band, and the operations in terms of square root, division, and arctangent are drastically reduced by 50%, 33%, and 50%, respectively. In addition, the proposed system only costs $474 USD and can serve as a suitable solution for various EIS applications in the future.

S19.3 | 11:00—11:15

A Power-Performance Aware Multi-Voltage Multi-Mode Video Encoder Implementation And System Validation

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This paper presents a low-power intra video encoder design using Multiple Voltage (Multi-Vdd) technology. Our design uses multiple supplied voltages to reduce power consumption without performance degradation. In this low-power encoder design, critical functional blocks operate at high voltage levels while non-critical blocks operate at low voltage levels. Front-end design techniques for voltage domain assignment optimization and back-end design techniques for die area with voltage-drop balance techniques are adopted to design this chip. This video encoder chip demonstrates that the Multi-Vdd technique can efficiently reduce power consumption without causing delays in circuit operations or increasing the die's area. A Hierarchy Multiple-Voltage (HMulti-Vdd) design technique is proposed in this paper to effectively reduce power consumption. This paper presents an EDA automation design flow that facilitates the separation of high-voltage and low-voltage modules during the synthesis stage. The proposed HMulti-Vdd methodology can be utilized to identify the optimal number of voltage domains and supplied voltage levels for designing a low-power chip while including performance estimation. The HMulti-Vdd software tool includes a low-power multi-Vdd chip design optimization process and integrates with several commercial circuit synthesis and physical design tools. Using HMulti-Vdd, the designed module voltage assignment is based on power, delay-time, and gate-count analysis. HMulti-Vdd can help designers reduce manual efforts in Multi-Vdd design. Several designed chips have been validated using this tool, showing that power consumption can be effectively reduced by up to 50%, with performance loss controlled within 5%. For system integration of the encoder chip, it has been successfully validated after system integration and has shown a 30% reduction in power consumption, which is better than the performance from the same design using a single supply voltage.