Oral S18

RF/Analog Circuits and Systems

Date/Time	8/4(五) 10:30—11:30
Chair(s)	鄭光偉／國立成功大學電機工程學系 張錦法／國立彰化師範大學電子工程系

S18.1 | 10:30—10:45

28 GHz VCO Using Magnetically Tuning Trifilar Transformer for Flicker Noise Up-Conversion Suppression

Chao-An Shen, Tai-Jung Hsu, and Kuang-Wei Cheng
National Cheng Kung University

This paper introduces a novel Voltage-Controlled Oscillator (VCO) using a magnetically tuned trifilar transformer to effectively suppress flicker noise up-conversion. By utilizing the feedback from primary and secondary coil of trifilar transformer, resulting in low supply voltage and large output swing. Consequently, the proposed design achieves low power consumption and low phase noise. By designing size ratio of primary and secondary resonators to a specific value can suppress flicker noise up-conversion. The tertiary coil of trifilar transformer is utilized to tune the VCO frequency. Particularly, this tuning process only requires a single control voltage, and the size ratio of primary and secondary resonators can be maintained during the tuning process. Additionally, a wider tuning range is achieved by applying different bias voltages to the center tap of the tertiary coil of trifilar transformer. The proposed 28.3 to 31.6 GHz VCO is fabricated in TSMC 40nm CMOS process and achieves -98.0 dBc/Hz at 1 MHz offset, while operating at a 0.6 V supply. The power consumption is 5.25 mW, and FoM is -181.73 dB.

S18.2 | 10:45—11:00

A 1-3 GHz Fast-Locking PLL Using Phase Injection With Multiplexed Ring Voltage-Controlled Oscillator in 90-nm CMOS

Hao-Cheng Hsu and Ching-Yuan Yang
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A 1-3GHz fast-locking phase-locked loop (PLL) using a phase injection technique to reduce the settling time of the PLL is presented. This paper proposes a novel approach to overcome the cycle slip issues occurring at phase transitions of +2π, -2π, +4π, and -4π, etc in traditional phase frequency detectors. By introducing a nonlinearity in the

phase detection process, the proposed nonlinear phase frequency detector (NPFD) demonstrates significant improvements in cycle slips issue. After frequency locking, utilizing a multiplexed ring voltage-controlled oscillator (MRVCO) and injecting a reference clock to compensate for accumulated phase errors during the tracking phase.

The proposed method can effectively reduce the time required for the PLL to lock onto the desired frequency. Additionally, this compensation mechanism effectively eliminates the accumulated phase error, resulting in a significant reduction of the PLL settling time by more than 50%. Fabricated in 90-nm CMOS technology. The reference clock frequency is 50MHz and the output frequency of the PLL ranges from 1 GHz to 3 GHz. When this PLL is switched from 1 GHz to 3 GHz, the settling time is 0.7us which is around 35 reference clock cycles. The root-mean-square jitter is 1.63ps. The power consumption of the PLL is 15mW at 3 GHz for a supply of 1.2V.

Keywords: Multiplexed ring voltage-controlled oscillator (MRVCO), Phase-locked loop (PLL), Phase injection, Nonlinear phase frequency detector (NPFD).

S18.3 | 11:00—11:15

A 433-MHz Class-E Power Amplifier with Adaptive Duty-Cycle Control and Precharge Mechanism

Chen-Hsing Hsu, Min-Hua Chang, Liu-Xin Yang and Yu-Te Liao
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This paper presents an energy-efficient 433 MHz wireless transmitter with burst-chirp modulation. To compromise the design trade-offs between output power and power consumption, the transmitter (TX) adopts a duty-cycle controlled class-E power amplifier (PA), whose switching dutycycle ratio is less than 50%. Through this method, the impedance transformation ratio at the output of the PA is reduced, thus improving efficiency. Furthermore, a digital controller directly modulates the oscillator, generating chirp pulses. Moreover, the precharge mechanism is proposed to improve settling time, allowing short-pulse data transmission time. The TX IC is fabricated using 180-nm CMOS technology and occupies an active area of 1.73 mm2. The design achieves 8.71/Mbit normalized system efficiency, while the output power is -1.18 dBm at a 0.8-V supply, and the maximum system efficiency is 45%.

S18.4 | 11:15—11:30

Design of A Novel Multi-Threshold Threshold Logic Gate Using Λ-Type MOS-NDR Circuit

Jia-En Hu and Kwang-Jow Gan
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In this paper, we present a design of a novel multi-threshold threshold logic gate (MTTG) circuit using the negative-differential-resistance (NDR) circuits which are composed of various MOSFET devices. The I-V characteristic curve of this MOS-NDR circuit shows a novel Λ-type feature. The operation of this MTTG circuit is based on the theory of monostable-bistable transition logic element (MOBILE), which utilizes the NMOS devices to control the switch operation of the NDR circuit in the input stage, thereby modulating the I-V characteristic curve of the entire circuit. We demonstrate a combinational logic y=(X1X2^'+X2) X3' with three inputs. This architecture can be used to implement programmable logic outputs. The difference between this MTTG architecture and traditional CMOS logic circuits is that this MTTG circuit can realize different logic functions without changing the overall circuit structure. We only need to design and adjust the parameters of MOS-NDR circuits.