Oral S16

Oversampling Data Converters

Date/Time	8/4(五)　10:30—11:30
Chair(s)	李大輝／南台科技大學電子工程系 陳佳宏／國立陽明交通大學電機工程學系

S16.1 | 10:30—10:45

A Discrete-Time Delta-Sigma Modulator for Audio Applications

Hou-Hsuan Lin and Yung-Hui Chung
National Taiwan University of Science and Technology

This work presents a second-order discrete-time (DT) delta-sigma modulator (DSM) for audio applications. By adding multiple feedforward paths in the cascade of integrators with feedback (CIFB) topology, the integrator output swing can be greatly reduced. Thus, the proposed DSM architecture can effectively reduce the dc gain of the operational transconductance amplifier used in the integrator. In addition, combining the passive adder and quantizer into a 4-bit SAR ADC can further save more power while increasing the resolution of the proposed quantizer. The prototype DT-DSM is fabricated in 180- nm CMOS technology and occupies an active area of 0.54 mm2. At 3.2-MS/s, this prototype ADC consumes a total power of 0.851 mW from a 1.8-V supply. With an oversampling ratio of 64, the signal bandwidth is 25 kHz. Measured SNDR and SFDR are 89.3 dB and 102.5 dB, respectively. The measured dynamic range is 90 dB. The equivalent Schreier figure of merit (FOMs) is 163.9 dB.

S16.2 | 10:45—11:00

A 91.7-dB SNDR Discrete-Time Zoom ADC with a 20-kHz BW in 180-nm CMOS

Zi-Chi Lin, Pei-Hsiu Kao, and Yung-Hui Chung
National Taiwan University of Science and Technology

This work presents a discrete-time zoom analog-to-digital converter (ADC) to achieve a 20 kHz bandwidth. The zoom ADC architecture combines a coarse successive-approximation register (SAR) ADC with a fine delta-sigma modulator (DSM) in a two-step way to maintain high resolution but less circuit complexity compared to traditional multi-bit DSMs. The prototype ADC is fabricated in a 180-nm CMOS technology. At 6-MS/s, it consumes a total power of 1.57 mW from a 1.8-V supply. The measured SNDR is 91.7 dB with a 20 kHz bandwidth and the resultant Schreier figure of merit is 162.7 dB.

S16.3 | 11:00—11:15

A Second Order CT DSM Hybrid 6-Bit SAR ADC with Sharing DAC for Bluetooth Applications

Yu-Wei Yang[1], Hung-Chi Chang[1], Hsin-Liang Chen[2], Jen-Shiun Chiang[1]
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This paper presents a low-cost, high-resolution continuous-time delta-sigma modulator (CT-DSM) for Bluetooth communications in an industrial 4.0 environment. The proposed architecture is a second-order CT-DSM that employs a 6-bit successive approximation register analog to digital converter (SAR ADC) as the quantizer with characteristics of high dynamic range and low power dissipation. In addition, a resistive digital-to-analog converter (DAC) is used to share the DAC between the modulator and the SAR quantizer, which can reduce area requirements. A prototype was designed and simulated by the TSMC 180-nm CMOS process. It achieves a 13-bit resolution with a bandwidth of 500kHz, and the power dissipation is 12.68mW.

S16.4 | 11:15—11:30

A Low-OSR 5th-Order Noise Shaping SAR ADC in a Two-Amplifier EF-EF-CIFF Structure with Low-Noise PVT-Robust V-T-V Converters

Bao-Shu Liu and Chih-Cheng Hsieh
Department of Electrical Engineering, National Tsing Hua University

This paper presents a low-OSR 5th-order noise-shaping SAR (NS-SAR) ADC with a low-noise Voltage-Time-Voltage (V-T-V) converter. It proposes an innovative EF-EF-CIFF structure that realizes fifth-order noise shaping using only two amplifiers. The proposed V-T-V converter is used to support all amplification with low noise and power. It enables a robustly optimized NTF without the cost of static-power amps and does not require any gain calibration or trimming bank for the noise transfer function (NTF), which reduces circuit complexity and power consumption. The prototyped ADC was fabricated in a 40nm CMOS process with an active area of 0.059mm2. At a supply voltage of 1.1V and a sampling rate of 5MS/s, it achieves an SNDR of 85dB over a 500kHz bandwidth. The resultant Schreier figure of merit (FoM) is 181.8dB, and the Walden FoM is 6.4fJ/conversion-step.