Oral S15

Testing, Reliability and Yield Enhancement

Date/Time	8/3(四)　11:30-12:30
Chair(s)	呂學坤／國立台灣科技大學電機工程學系 謝東佑／國立中山大學電機工程學系

S15.1 ｜ 11:30—11:45

Localized Fault-Tolerant TSVs using Differential Signaling For Multi-Vendor 3D-IC Design Environment

Ching-Yi Wen, Shi-Yu Huang
Electrical Engineering Department, National Tsing Hua University

A faulty Through Silicon Via (TSV) could spoil a 3D IC and cause hefty loss as the potentially expensive known-good-dies bonded together will have to be discarded. This work presents a fault-tolerant scheme uses two differential TSVs for binary signal transmission. Compared to prior fault-tolerant TSV schemes, our test and repair protocol is much more simplified and without global test result analysis and complex reconfiguration, making it especially suitable for a cooperative multi-vendor 3D-IC design environment.

S15.2 ｜ 11:45—12:00

On Cost-Effective Extending Tolerable Error Rates of DNN Memory: A New Protection Method and A Case Study on YOLOv4

Wei-Ji Chao and Tong-Yu Hsieh
Department of Electrical Engineering, National Sun Yat-sen University

In the context of Deep Neural Network (DNN) computing, memory errors may occur and accumulate due to a variety of factors, such as defects, aging or even the usage of low-power technologies. As a result, it is critical to protect DNN memory in a cost-effective manner. However, previous memory protection methods have difficulty in dealing with high memory error rates. In this study, we investigate the inherent error tolerability of memory errors of various rates of DNN by considering YOLOv4 as a case study. We also analyze the effectiveness limitation of previous error mitigation techniques. Building on these analyses, we propose a novel memory protection method that can tolerate high error rates without compromising DNN accuracy. The experimental results show that our method only causes a 1% decrease in DNN accuracy even at error rates as high as

0.1%, which is a significant improvement over the state-of-the-art techniques. In addition, our method incurs a comparable cost overhead.

S15.3 | 12:00—12:15

Error Mitigation Techniques for Flash Memory of DNN Accelerators

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National Taiwan University of Science and Technology

Deep neural networks (DNNs) are being widely used in smart appliances, face recognition and autonomous driving. The trained weight data are usually stored in flash memory which suffers from reliability and endurance issues. Owing to the inherent error tolerability for DNN applications, address remapping techniques are proposed for protecting weight data stored in flash memory. Bit significances are first analyzed and then a weight transposer is proposed for remapping significant weight bits to fault-free or much reliable flash cells. A bipartite graph model is developed for modeling address remapping. The corresponding hardware architectures for address remapping are also proposed. Experimental results show that based on 0.01 % injected BER in the weight data, the accuracy losses of widely used DNN models are less than 1% with negligible hardware overhead.

S15.4 | 12:15—12:30

Software-Based Self-Test for Processor Register File

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[3] Department of Electrical Engineering, National Taiwan University

Software-based self-testing (SBST) is a promising technique to ensure processors' reliability after deployment. During SBST, the processor under test executes tailored self-test programs to activate faults and capture test responses. One limitation of SBST is that the achievable fault coverage is generally lower than that of scan-based testing. To improve SBST fault coverage, this paper proposes a test program template for the processor's register file circuit. Based on the template, the generated algorithmic test program is more efficient, in terms of fault detection capability and test program size, than those converted from ATPG test patterns. Furthermore, the template also reduces the whole-processor test program generation efforts. The proposed technique is validated on a RISC-V processor. It improves the whole-processor transition delay fault coverage by 3.43% and test program generation time by 28.6%.