Oral S12

PLLs, DLLs and Wireline Transceivers

Date/Time	8/3(四)　11:30-12:30
Chair(s)	翁峻鴻／東海大學電機工程學系 洪振傑／逢甲大學電子工程學系

S12.1 ｜ 11:30—11:45

A 3.4-Gb/s Adaptive Equalizer with Wide Input Common Mode Range for TFT-LCD Interfaces

Ming-Yan Xu and Soon-Jyh Chang
Department of Electrical Engineering, National Cheng Kung University

This paper presents a 3.4-Gb/s adaptive equalizer with a wide input common mode range for large display panels interface. We propose an equalizer filter that can operate with a wide input common mode range from 0.3-V to 1.2-V without degrading the high-frequency boosting and input swing ranges. In addition, by adopting the swing control technique, the unbalancing-swing problem can be avoided. The measured jitter of 3.4-Gb/s and 1.0-Gb/s data are 0.32-UI and 0.1-UI for the 1.4-m FR4 board, respectively. Fabricated in a 0.18-μm CMOS process, the core area occupies 0.185 mm2 and the power consumption is 29.4-mW at 3.4-Gb/s from a 1.8-V supply.

S12.2 ｜ 11:45—12:00

A Low Power 16-Gbps CTLE and Quarter-Rate DFE with Single Adaptive System

Chun-Yao Chang, Yun-Teng Shih and Kuo-Hsing Cheng
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This article presents a low power 16-Gbps equalizer with single adaptive system. A novel equalizer architecture relaxes the timing constraint of decision feedback equalizer (DFE) from one period to two period. Thus, we may utilize low power techniques to realize DFE to reach better power efficiency. The data path is composed with continuous time linear equalizer (CTLE) and 2-tap DFE for lower hardware area. To achieve lower bit error rate (BER), sign sign least-mean-square (SS-LMS) algorithm is adopted to provide optimum gain of CTLE and tap weight of DFE simultaneously. This chip is fabricated with TSMC 90 nm (TN90GUTM) 1P9M CMOS process and occupies an active area of 0.047 mm2. The proposed adaptive equalizer may compensate for the channel loss up to 16 dB at 16 Gb/s. The power consumption is 4.24 mW from 1.0V supply, and achieve the figure of merit of 0.265 mW/Gbps.

S12.3 | 12:00—12:15

A 0.6-V 3.48-mW 2.5-GHz Frequency Synthesizer With Pulse-Width to Current Conversion

Peng yun and Ching-Yuan Yang
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In this paper, a 2.5-GHz frequency synthesizer using a pulse-width to current conversion (PWCC) circuit is presented. The proposed PWCC technique converting the pulse-width of input clock signal into a modulated output current is applied to improve the conventional charge-pump. Implemented by TSMC 90 nm CMOS process, the proposed frequency synthesizer dissipates 3.48mW from a 0.6-V power supply. The operation frequency is from 2.32GHz to 2.66GHz under the channel width of 1 MHz. The measured output spurious tone is -52.2 dBm and the phase noise performance is -100.52dB/Hz at 1MHz and -125.61 dB/Hz at 10 MHz offset from carrier frequency of 2.4GHz.

S12.4 | 12:15—12:30

Digital Delay Locked Loop with Monotonic Delay Line

Jen-Chieh Liu, Chuan Yang, and Ke-Nan Lin
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This paper proposes a digital delay locked loop (DLL) with a monotonic delay line. This DLL adopts the calibration mode to reduce the non-monotonic effects for the coarse-tuning delay line (CTDL) and the fine-tuning delay line (FTDL). The calibration mode detects the delay time of the delay unit, the timing resolution of the CTDL, to adjust the delay range of the FTDL. Thus, the calibration mode can limit the overlap range of the delay time between the CTDL and the FTDL. The proposed DLL was implemented by a 0.18 μm CMOS process and the RMS and the peak-to-peak jitters of the DLL are 0.21% and 1.72%, respectively, at 560 MHz. The power consumption is 8.82 mW at 560 MHz.