Oral S11

Nyquist-Rate Data Converters

Date/Time	8/3(四) 11:30-12:30
Chair(s)	張裕鑫／國立虎尾科技大學電子工程系 宋國明／國立台北科技大學電機工程學系

S11.1 | 11:30—11:45

A 12-Bit Three-Step Cyclic Time-to-Digital Converter with Calibrated Timing Window Using the Dual-Mode Pulse-Shrinking-Locked Loop

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This paper presents a 12-bit three-step cyclic time-to-digital converter (TDC) for biosensor devices and interface circuits. A dual-mode pulse-shrinking delay line (DMPSDL) is proposed to reconfigure the timing window in the delay line. A single set of timing circuits is shared between coarse and fine cyclic steps. Moreover, no external precise clock is required as a reference. The proposed TDC achieves high resolution and wide dynamic range at the same time. This design is implemented in TSMC CMOS 0.35 μm technology and the conversion rate is 100 kS/s. The measurement results show a wide dynamic range of 102.4 ns. The integral non-linearity (INL) and differential non-linearity (DNL) are -0.34 to 0.29 LSB and -0.81 to 0.86 LSB, respectively. With a power consumption of 1.18 mW, the figure of merit (FoM) for each conversion step is 5.41 pJ/conversion step.

S11.2 | 11:45—12:00

A 10-bit Successive-approximation ADC Design Based on Separate Comparison Techniques

Mao-Jung Huang, Li-An Tsai, Yi-Zhen Chen, and Po-Yu Kuo
Department of Electronic Engineering, National Yunlin University of Science & Technology

This paper presents a SAR ADC ultrasound detection device (UDD) utilizing the MSB and LSB separate comparison techniques (MLSCT). Through MLSCT the variation of input common-mode voltage for the comparator is effectively reduced, thereby increasing its yield. The proposed SAR ADC is implemented in 180nm CMOS processes, respectively. In the proposed SAR ADC, the measured SNDR, SFDR, and ENOB are 56.31 dB, 66.42 dB,

and 9.02 bits when the sampling rate is 10 MS/s and the supply voltage is 1.8 V, respectively. The proposed SAR ADC only consumed 0.831 mW.

S11.3 | 12:00—12:15

A 12-BIT 150MS/S PIPELINED-SAR ADC WITH LOW DC GAIN AMPLIFIER

Hung-Po Kuo, Ssu-Lei Tu and Chih-Cheng Hsieh
Department of Electrical Engineering, National Tsing Hua University

This paper presents a 12-bit 150MS/s pipelined successive-approximation register (SAR) analog-to-digital converter (ADC) with a low DC gain operational amplifier (opamp) using a dual-residue technique. By the dual-residue technique, the reference voltage used for the next stage will be generated and combined with residue voltage, and both of them are amplified, which achieves automatic reference-scaling. As a result, the finite gain error can be ignored while the DC gain requirement of opamp can also be relieved, which can resolve the problem of smaller intrinsic gain of devices in advanced process and decrease the design complexity and power consumption of opamp. The prototype was fabricated in 40nm 1P9M CMOS technology with a core area of 0.092 mm2.

S11.4 | 12:15—12:30

A 10-Bit 200-MHz Switched-Current Pipelined Analog-to-Digital Converter for Very-High-Bit-Rate Digital Subscriber Line

Guo-Ming Sung, Ming-Chang Tsai, Bo-Heng Zhou, Yu-Min Yu, and Chih-Ping Yu
Department of Electrical Engineering, National Taipei University of Technology

This paper proposes a 10-bit 200-MHz switching-current (SI) pipelined analog-to-digital converter (ADC) for very-high-bit-rate digital subscriber line (VDSL). The proposed pipelined ADC is composed of a 9-stage architecture, which includes eight 1.5-bit pipelined architectures and a 2-bit flash architecture at the last stage, to complete a 10-bit pipelined ADC. In addition, a digital correction circuit is used to eliminate the error generated by comparator and an active return current mirror is considered not only to reduce the input impedance but also to relax the channel-length modulation effect. The proposed pipelined ADC is designed and implemented in TSMC 0.18-μm 1P6M process. According to the simulated results, the SNDR, ENOB, DNL, INL, and power consumption are 57.447 dB, 9.25 bits, 1.002 LSB, 0.936 LSB, and 66.258 mW, respectively, at a supply voltage of 1.8 V and an input current in the range of −40 to +40 μA.