Oral S10

Communication, Automotive, and Low-Power Electronics

Date/Time	8/2(三)　15:30-17:00
Chair(s)	夏勤／長庚大學　機械工程學系 林進發／朝陽科技大學　資訊與通訊系

S10.1 ｜ 15:30—15:45

Layout Design and T-shaped Gate Metal to Improve RF Performance of Stacked Nanosheets/Nanowires

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The double-sided gate contact (DS) and contact over active-gate (COAG) layouts with and without T-shaped gate metal are studied by TCAD simulation considering stacked nanosheet (NS) and nanowire (NW) transistors. DS layout with gate contacts at both sides of the active region suffers from large gate resistance (Rg) and low maximum oscillation frequency (fMAX) as the gate finger width increases. COAG with additional gate metal vias on the active region can reduce Rg to improve fMAX but increase the parasitic capacitance (Cpar) to degrade the cut-off frequency (fT) under large gate finger width. T-shaped gate metal can further reduce the Rg due to less portion of high resistivity work-function (WF) metal. Stacked NW can achieve the highest fT=590GHz and the highest fMAX=830GHz considering the DS layout with T-shaped gate metal to reduce Rg, suitable for B5G and 6G wireless applications.

S10.2 ｜ 15:45—16:00

Design and Implementation of Hierarchical Space-Time Beam Search in Hybrid-Beamforming MIMO-OFDM Systems

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Millimeter wave (mmWave) multiple-input and multiple-output (MIMO) hybrid-beamforming systems are essential to deliver high throughput for recent wireless communications. However, the system performance relies heavily on beamforming gain. Thus beam training and beam search are critical to establish the communication link. A

hierarchical beam search procedure is designed and implemented for wideband communication systems. In the beginning, multiple beams in the upper layer of a hierarchical codebook with aggregate coverage approaching omni-directional radiation pattern are used for packet detection. Then, PN-sequence is transmitted and the beam patterns in lower layers are utilized for further refinement to strike a good balance for performance and search complexity. A space-time beam search procedure is employed to distinguish the angle-of-arrival (AoA), angle-of-departure (AoD) and delay of each path. The corresponding hardware is also implemented. From simulation results, the accuracy of space-time beam search is demonstrated and the efficiency brought by hierarchical search can also be shown.

S10.3 | 16:00—16:15

Hybrid SCF/SCAN Decoding for Polar Code

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Polar has lower coding and decoding requirements, linear complexity, and superior channel performance, so it is proven to be close to the Shannon limit for 5G communication. SC is a polar code decoding method, but its performance has a lot of room for optimization, flip methodology is a basic optimization. SCF has a good error correction capability, but it has a very long latency due to the repetition of SC decoder during computation. SCF output is only hard decision, so it cannot be used in soft input and soft output. To allow SCF to be used in more decoding environments, the Hybrid SCF/SCAN proposed in this paper can freely select soft output and hard output, and this architecture can reduce the problem of repeatedly computing SC decode.

S10.4 | 16:15—16:30

A Convolutional Hyperdimensional Computing Framework for LiDAR-based Place Recognition

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Place recognition is an important task for simultaneous localization and mapping (SLAM) systems. Place recognition algorithms are essential to analyze information collected from previously visited locations while correcting errors that may have occurred during map construction due to intrinsic noise in the sensor data and over time. Recently, the

adoption of LiDAR-based place recognition algorithms in real-world navigation has been steadily increasing due to their ability to resist the impact of external lighting changes and maintain a higher level of stability. However, there is a lack of focus on the storage and search costs associated with storing features in memory, which is becoming increasingly significant as the field continues to evolve. Managing the amount of stored data is particularly crucial as the volume of information expands rapidly over time. In this work, we propose a Convolutional Hyperdimensional Computing (CHDC) framework to address the above problems, and we introduce a binary quadruplet loss for training binary feature representation. Based on the experiments, our CHDC-10000d solution improves F1-score by 1.4% and has a 1.9× speedup compared with previous methods on the KITTI dataset on Raspberry pi 4. To further improve search time, the CHDC-1024d solution achieves 13.5× speedup with only a 1.6% F1-score drop.

S10.5 | 16:30—16:45

A Digital Design Flow for Mos Current-Mode Logic

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In this paper a digital design flow for implementing MCML circuits is presented. MCML circuits are fully differential and are not directly supported by commercial CAD tools. A special design methodology must be developed such that design of MCML circuits can be automated using standard CAD tools. MCML standard cells are first designed and the required libraries required for commercial CAD tools are then generated. Synthesis and place & route (P&R) in a single-ended domain that tricks commercial CAD tools as treating MCML circuits as standard CMOS logic circuits. An algorithm that automatically converts single-ended circuits into fully differential MCML circuits is developed. After validation of the design flow, a 100-MHz sigma-delta modulation DAC was taped out using UMC's 0.18um process. Unlike previous works on MCML design automation, this work ended with a real fabricated chip, where lots of effort were put in to resolve density and large scale DRC problems.

S10.6 | 16:45—17:00

A Low Power and Area Efficient Sense-Amplifier Based Flip-Flop Design

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A novel low power and area efficient sense-amplifier(SA) based flip-flop (FF) for low power applications is proposed. The proposed design successfully combines both sense amplifier design and latch design, thereby reducing the area and addressing the additional power consumption caused by glitches in the previous SAFF designs. These factors improve the power consumption and the power-delay-product of the design substantially and the performance claims are verified through extensive post-layout simulations.