Oral S09

Learning Based Frameworks in EDA

Date/Time	8/2(三)　15:30-17:00
Chair(s)	鄭維凱／中原大學資訊工程學系 劉一宇／國立臺灣科技大學資訊工程學系

S09.1 | 15:30—15:45

Multi-Corner Timing Macro Modeling with Neural Collaborative Filtering from Recommendation Systems Perspective

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Timing macro modeling has been widely employed to enhance the efficiency and accuracy of parallel and hierarchical timing analysis. Several algorithmic and machine learning-based approaches have been proposed to achieve accurate and compact timing macro models. However, prior work primarily focused on single-corner libraries, making it difficult to adapt these approaches to multi-corner situations. This either incurs substantial engineering effort or results in significant performance degradation. To tackle this challenge, we offer a fresh perspective on the timing macro modeling problem by drawing inspiration from recommendation systems and formulating it as a matrix completion task. We propose a neural collaborative filteringbased framework capable of capturing the convoluted relationships between circuit pins and timing corners. This framework enables the precise identification of timing variant regions across different corners. Additionally, we design several training features and implement various training techniques to enhance precision. Experimental results show that our framework reduces model sizes by more than 10% compared to state-of-the-art single-corner approaches, while maintaining competitive timing accuracy. Moreover, our framework exhibits significant improvements in runtime. Furthermore, when applied to unseen corners, our framework consistently delivers superior performance, demonstrating its potential for utilization in off-corner chiplets.

S09.2 | 15:45—16:00

ML-CELLO: Machine Learning-Driven VLSI Cell Layout Optimization with Layout Dependent Effects

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This work proposes a new approach that combines an existing layout generator with a machine learning-based evaluation flow to enable rapid performance ranking of standard cells in VLSI circuits. This model incorporates layout dependent effects (LDEs) in feature extraction, generating an ordered list of cell layouts, and evaluating only the top-K candidates for performance. The experiments show that this approach successfully identifies the optimal layout from 10 benchmark cells in a sub-5nm FinFET industrial standard cell library, achieving a 348x speedup over the conventional flow. This approach offers a promising alternative to traditional optimization techniques, which rely on metrics that fail to capture actual performance.

S09.3 | 16:00—16:15

Dynamic IR-drop Prediction of At-speed Two-vector Tests Using Machine Learning

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—Excessive dynamic IR-drop in VLSI testing causes timing violations, which leads to test failure. The dynamic IR drop becomes a more serious problem in at-speed two-vector tests than that in stuck-at tests due to the at-speed clock. However, we need Machine Learning methods to speed up the analysis because of the long runtime of dynamic IR-drop analysis. In this paper, we propose two new methods to predict dynamic IR-drop of at-speed two-vector tests. One uses two models for the first capture cycle and the second capture cycle, respectively. The other one combines features of two capture cycles. Also, we propose spaced window features and time-sliced features to improve prediction accuracy. Our mean absolute error for the worst dynamic IR drop prediction is 5.230mV, which is less than 0.6% of the supply voltage. Our experiment results show at least a 12.6X speed-up ratio compared to a commercial tool. With our technique, we can identify two-vector tests which have excessive IR-drop in a short time to prevent yield loss.

S09.4 | 16:15—16:30

PVT-Sensitive Delay Fitting for High-Performance Computing

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Aggressively monitoring and tracking system-on-chip (SoC) performance under process/voltage/temperature (PVT) variations is essential for high-performance computing systems. This work observes that different chips of the same SoC design may have different PVT-to-delay sensitivities, which must be carefully considered for accurate chip performance tracking. A learning-based method is then proposed to fit critical path delay for different chips with different PVT-to-delay sensitivities. Experimental results based on the fabricated chip samples of a 7nm SoC have justified the effectiveness of the proposed PVT-sensitive delay fitting method. Compared with the state-of-the-art, our method can achieve excellent performance tracking accuracy when the chip performance is dominated by different critical paths under different PVT conditions.

S09.5 | 16:30—16:45

An Efficient and General Multi-Level Framework for Distributed Acceleration

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Driven by the scaling of advanced technology nodes and the growing design complexity, the relentless progression of integrated circuits and systems poses a significant challenge to large-scale scheduling for applications/workflows in modern design. Current scheduling techniques fall short of effectively managing this burgeoning complexity and utilizing additional computing resources for scalability. This paper proposes a multi-level framework tailored to optimize makespan, taking into account machine synchronization costs and computing resource utilization. The proposed approach primarily focuses on constraint satisfaction through the utilization of a constraint-aware recomposition technique during the uncoarsening phase. Additionally, from a global perspective, a dynamic programming (DP)-based optimization strategy is employed to enhance the overall solution quality in accordance with user-defined objectives during the coarsening phase. Comprehensive experimental evaluations are

conducted on timing analysis circuits, sum-product networks commonly employed in machine learning tasks and directed acyclic graphs (DAGs) in scientific computing applications, demonstrating that our method outperforms existing state-of-the-art techniques in terms of makespan, exhibiting significant improvements in scalability, both in relation to problem size and the number of machines. Moreover, the ability to handle general DAG scheduling instances reveals the practical value and effectiveness of our framework in accelerating computation.

S09.6 | 16:45—17:00

Camouflaged Cell-Based Security-Driven Timing ECO Algorithm

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Gate camouflaging is an effective method for protecting integrated circuits (ICs) against reverse engineering attacks. However, the integration of camouflaged gates may introduce timing violations. To address this issue, we propose a metal-only timing ECO (engineering change order) method that leverages camouflaged cells as spare cells and replaces normal cells with camouflaged cells during the timing ECO process. The proposed timing ECO algorithm consists of two stages: the first stage focuses on rectifying timing violations while enhancing security, and the second stage leverages timing slacks to further maximize security. Through the efficient utilization of camouflaged cells, experiment results show that our approach can mitigate the risk of reverse engineering attacks while maintaining circuit performance.