# Oral S08

## Multi-core Systems, Network on Chip, and Embedded SOC Systems

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| Date/Time | 8/2(三)　15:30-17:00 |
| Chair(s) | 陳冠宏／逢甲大學電子工程學系<br>吳志峰／長庚大學電子工程學系 |

### S08.1 | 15:30—15:45

**Edge and Trustworthy AI System Design based on FPGAs for Air Quality Monitoring**

*Chun-Hsian Huang, Yi-Chun Chang, Wen-Tung Chen, Kuan-Ting Wu and Ren-Hong Wang*
*Department of Computer Science and Information Engineering, National Taitung University*

This work presents an edge and trustworthy AI system design based on FPGAs, which contains a neural engine that can execute our customized AI model for air quality index (AQI) level classification and a pre-trained model for detecting objects containing private information. Furthermore, the proposed design incorporates a de-identification process, cryptographic functions and protection matrices to safeguard information and individuals' privacy. Cryptographic functions and protection matrices are implemented as reconfigurable modules, which can accelerate processing and protect data privacy and be reconfigured as needed. Compared to the embedded GPU solution, the proposed design can achieve a speedup of 4.7x for AQI level classification, while it can enhance energy efficiency by 5.02x. To support all the cryptographic functions and protection matrices, system adaptivity can significantly increase resource utilization while decreasing power consumption by up to 2.79% in terms of the Zynq UltraScale+MPSOC XCZU19EG chip.

### S08.2 | 15:45—16:00

**LASSO-based Thermal Sensor Placement for the Temperature-aware Multi-core System**

*Kun-Chih (Jimmy) Chen[1] and Lei-Qi (Laichi) Wang[2]*
*[1] Institute of Electronics, National Yang Ming Chiao Tung University*
*[2] Department of Computer Science and Engineering, National Sun Yat-sen University*

While multi-core systems have significantly improved performance compared to single-core systems, they have also increased the complexity of system design, leading to a

large number of complex calculations and resulting in severe temperature issues. These temperature problems not only reduce system performance and reliability but also affect the lifespan of the chips. The placement of sensors in appropriate positions within a limited quantity, while effectively monitoring temperature and considering hardware costs, presents a major challenge. In light of these challenges, many research studies have proposed methods for sensor placement, such as greedy algorithms, and principal component analysis. Although these methods have shown promising results, they still have issues such as the inability to handle nonlinear data or high computational complexity. To address the need for reducing computational complexity and properly selecting suitable sensor locations, we propose a sensor placement method based on the Least Absolute Shrinkage and Selection Operator (LASSO). LASSO is a regularization technique that can efficiently handle high-dimensional data and select valuable features, making it easier to achieve high sparsity at low computational complexity. In summary, our goal is to reduce computational complexity and quickly obtain appropriate sensor placement locations. The proposed technique based on LASSO fulfills these objectives and achieves better placement results. According to the experimental results, we can reduce the average reconstruction error by 10%-78% and the maximum reconstruction error by 2%-81% compared with other related works.

S08.3 | 16:00—16:15

### Jitter Minimization of a Cell-Based PLL with a Linearized DCO

*Yi-Sheng Wang, Hsiang-Kai Teng, Shi-Yu Huang*
*Electrical Engineering Department, National Tsing Hua University*

A cell-based Digitally Controlled Oscillator (DCO) is a key cell-based Phase-Locked Loop (PLL) component for on-chip high-speed clock generation. Previous cell-based DCO still suffers from some drawbacks such as nonlinear DCO period profile, non-uniform time resolution, risks of output clock period gaps, etc. In this work, we overcome these drawbacks by using latch-based varactor cells. Post-layout simulation reveals that our DCO can guarantee a gapless output clock period range for all 5 process corners in the most extreme temperature range from -40°C to 150°C. At the same time, the time resolution is stable at 1ps across the entire clock period range, leading to a peak-to-peak jitter reduction of our cell-based PLL.

S08.4 | 16:15—16:30

### Hybrid Data Transmission in NoC-based DNN Accelerator for Efficient Data Reuse

*Kun-Chih (Jimmy) Chen[1] and Hao-Xiang (Howard) Peng[2]*

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*[2] Department of Computer Science and Engineering, National Sun Yat-Sen University*

With the development and application of Deep Neural Networks (DNN) accelerators in recent years, it has become more efficient to perform neural network computations. Because of the different computing requirements, the data transmission in the target DNN model is different, which increases the difficulty of the DNN accelerator design. However, the dedicated array-based PE interconnection limits efficiency and data reuse computation methods, which increase memory access. It is difficult to design a suitable dataflow to support multiple data reuse methods based on array-based PE interconnection. On the other hand, data reuse methods such as input reuse and weight reuse have been extensively used in DNN accelerators to reduce memory access. These methods involve sending a single packet of data to multiple processing elements. However, due to the need for a large amount of one-to-many data transmission, traditional unicast transmission has been unable to efficiently transmit data. In this work, we propose a hybrid data transmission method and use Network on Chip (NoC) interconnection to address the aforementioned problems. The proposed mechanism can support various data transmissions (i.e., unicast, multicast, and broadcast) in DNN computing. Besides, the NoC-based DNN design provides a highly flexible transmission that leverages various data transmissions for the target DNN model. Our approach aims to reduce transmission latency and minimize the number of packets on the network. Compared with the related work, we can reduce the latency by 25% to 75% according to LeNet and AlexNet models because of efficient and hybrid data transmission method.

S08.5 | 16:30—16:45

### An Efficient TDNN Based Wake Up System SoC Using RISC-V Embedded Microcontroller

*Tsung-Han Tsai and Meng-Jui Chiang*

*Department of Electrical Engineering, National Central University*

The wake-up system is widely used in the daily life. It normally has highly constrained calculation resources due to the power consumption and chip area. In this paper, we propose an efficient model based on time-delay neural network (TDNN) for the wake-up system. The number of parameters in this model is less than 20K. The accuracy only decreases to 85% evaluated on "Hey Snips" dataset. We also implement the wake-up system on Andes AE350 platform with N25F RISC-V embedded microcontroller. The platform is synthesized in TSMC 90nm technical process with 0.9V power supply.

S08.6 | 16:45—17:00

### An Option Strategy based on Put–Call Parity

*De-Hao Zhao, Chih-Yu Lin, Yan-Chen Lin, Hsi-Pin Ma*
*Department of Electrical Engineering, National Tsing Hua University*

In collaboration with Vsense Fintech Inc., this paper presents a novel option buying and selling strategy and pricing method based on Put-Call Parity. By utilizing market options and futures spot prices, we calculate the theoretical option price. Additionally, we propose an improved binary search algorithm that replaces the integer divider in the strategy algorithm, reducing computation time by 2.6 times to accommodate low-latency trading systems. The strategy algorithm is implemented using High-Level Synthesis and executed on an FPGA. The results demonstrate less than 0.35% error from the market price within 112.5 ns, enabling quick decision-making on high and low points in option prices for efficient buying and selling.