Oral S07

Power and Driver Circuits

Date/Time	8/2(三)　15:30-17:00
Chair(s)	陳景然／國立臺灣大學電機工程學系 黃崇勛／國立中正大學電機工程學系

S07.1 | 15:30—15:45

Envelope-Tracking Based Dynamic Biasing Circuit for Power Amplifier

Po-Hung Lin, and Hsiao-Chin Chen
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An envelope-tracking (ET) based dynamic biasing circuit is designed and implemented using TSMC 180-nm CMOS technology for power amplifiers (PAs) in modern wireless communications with high peak-to-average-power-ratio. Based on the hybrid supply modulator, the dynamic biasing circuit consists of a wideband linear modulator, and a switching modulator. The circuit provides the output bias voltage from 1.5 V to 3.5 V for an input level from 1.5 V to 3.5 V. The output voltage of the circuit exhibits the ripple of 10.324 mVpp to 5.581 mVpp from 20 MHz to 100 MHz.

S07.2 | 15:45—16:00

Single-Inductor Bipolar-Output Converter with Tunable Power Distribution and Power-Efficient Skipping Control for AMOLED Application

Meng-Xun Cai, Wei-Ting Yeh, Chun-Yu Chen, Xuan-Fu Wu and Chien-Hung Tsai
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This paper proposes a single-inductor bipolar output (SIBO) boost converter with an adjustable synchronous load transient cross-regulation energy allocation strategy. The converter is designed as a solution for active-matrix organic light-emitting diode (AMOLED) pixel power management, supplying the necessary positive and negative voltages for AMOLEDs using only a single external inductor. To tackle the challenges of energy allocation imbalance and transient voltage overshoot caused by cross-regulation, we incorporate a tunable K mechanism in the power distribution control (PDC) loop. Furthermore, to ensure high-efficiency operation across a wide load range, we introduce an additional operating mode under light load conditions to reduce the switching frequency and improve power conversion efficiency. The proposed SIBO DC-DC converter is suitable for load ranges from 20mA to 200mA and is fabricated in a

0.18μm CMOS process. Experimental results confirm the effectiveness of the proposed tunable power distribution control, and the power conversion efficiency of the converter remains above 75% throughout the entire load range.

S07.3 | 16:00—16:15

High-speed CMOS Half-Bridge Gate Driver for GaN-Based DC-DC Converter

Xuan-Fu Wu, Wei-Ting Yeh, Chun-Yu Chen, Meng-Xun Cai and Chien-Hung Tsai
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This paper presents a novel gallium nitride (GaN) half-bridge gate driver designed for 5G telecom power and industrial power supplies in real-time microcontrollers. The proposed driver incorporates the advanced Dual-edge Delay-Locked loop Dead-time Control technique. In comparison to previous research efforts, this study introduces an additional VSW leading edge control loop. The primary objective of this enhancement is to prevent shoot-through occurrences and mitigate reverse conduction losses during dead-time intervals. Moreover, the system integrates CBST voltage control and Floating Level Shifters circuitry. The inclusion of CBST voltage control ensures the prevention of gate damage caused by CBST overcharging, while the implementation of floating level shifters guarantees signal accuracy during high-speed operations, thereby enhancing system reliability. The proposed driver IC is fabricated using an advanced 0.18μm BCD process to evaluate the effectiveness of the proposed control scheme. Measurement results demonstrate a significant reduction in reverse conduction time, resulting in a notable 7.5% efficiency improvement compared to the conventional fixed dead-time control at 0.3A.

S07.4 | 16:15—16:30

A 94.3 % Peak Power Efficiency Time-Based Buck Converter Using Pulse-Phase-Shift Modes with An Intrinsic Window for Transient Enhancement

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This paper proposes a time-domain controlled buck converter with fast transient response. The dual-mode control consisting of pulse-width modulation (PWM) and pulse phase shift-pulse train (PPS-PT) modes is utilized to suppress the voltage ripples during the steady state and enhance the transitions between the light and heavy load, respectively. The edge-pursuit comparator (EPC) is adopted to detect the voltage difference and decide the operation mode when the load varies. Compared with

conventional hysteretic window control, lower power consumption and better transient response are achieved. Measurement results show that when the load varies from 50 mA to 450 mA, the recovery time is 2.5 μs and the undershoot is 100 mV. The overall peak power efficiency is 94.3 % and a FoM of 1.68 mA*%/μs*mV is accomplished.

S07.5 | 16:30—16:45

A Current-Adaptive Input Driver for ADCs

Zu-Jia Lo, Ren-Yong Hung, Yun-Jie Huang, Tzu-Heng Hsu, Hsiu-Min Yang, Xiu-Zhu Li, Ting-Han Hsu, Yuan-Chuan Wang, Guan-Chun Fang, Sheng-Yu Peng
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This paper presents a power-efficient autonomous current adaptation input driver (ACAID) for analog-to-digital converters (ADCs) using floating-gate transistors for reconfig-urability. The ACAID autonomously adjusts the supply current during the tracking phase, achieving a high slew rate, and reduces the current during the RC-settling or hold phase to the original low quiescent level. The required sensing and actuating circuits for current adaptation are inherent in the capacitive feedback topology. A prototype version of the ACAID was designed and fabricated in a 0.35 μm CMOS process, achieving –70.1 dB THD with a 100 kHz input signal and 9.1 effective number of bits (ENoB) near the Nyquist rate with a 200 kHz sampling rate. The proposed ACAID achieves significant power savings at higher input frequencies or reduced tracking periods, with up to 76.2% power savings at a 1MHz sampling rate.

S07.6 | 16:45—17:00

High-Efficiency and Wide-Load Current Range LDO Regulator with Dynamic Loop Gain Control Technique

Yu-Lung Lo, Chia-Wen Lin, and Yu-Chun Chiu
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This paper proposes a low dropout regulator design with dynamic loop gain control for wide-load current range. It uses a multi-phase error detection mechanism, a tri-state damping selector, and a dynamic integration shift register to predict load variation and adjust loop gain for fast response and low power consumption. The design also lowers output voltage ripple to improve achieve high current efficiency.