Oral S05

Recent Advances in Physical Implementation

Date/Time	8/2(三)　13:30-15:00
Chair(s)	麥偉基／國立清華大學　資訊工程學系 林柏宏／國立陽明交通大學　智慧科學暨綠能學院

S05.1 | 13:30—13:45

Optimizing Package Designs: An Analytical Multi-die Floorplanner Considering Warpage Effects

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The mismatch in the coefficients of thermal expansion between different materials causes nonuniform deformation in a package, called warpage. The warpage effect has become a critical reliability issue still not well handled in advanced packaging. We present the first analytical multi-die floorplanning algorithm considering the warpage effect in advanced package designs. We develop a physical warpage model that can be embedded into a gradient-based floorplanner to optimize the warpage effect. We then present a warpage, wirelength, and area co-optimizer considering the overlapped region and outline barrier constraints. Simulation results justify the effectiveness of our warpage model, and experimental results show that our floorplanner outperforms TCG-based ones in warpage, wirelength, and area.

S05.2 | 13:45—14:00

STAR ONoCs: Provably Good Fault-Tolerant Topologies for Wavelength-Routed Optical Networks-on-Chip Designs

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The wavelength-routed optical network-on-chip (WRONoC) is a promising solution for advanced signal communication because of its high-bandwidth, low-latency, and power-efficient signal transmissions. Nonetheless, WRONoCs suffer from the issue of MRR failures, which need to be handled by developing fault-tolerant topologies. Existing

fault-tolerant WRONoC topology design flow relies on random-based algorithms with no quality or feasibility guarantee. To remedy this disadvantage, we present two fault-tolerant topologies, namely the Actin-STAR and Zygo-STAR topologies, with performance guarantees. We prove that the Actin-STAR topology has a performance bound of 2.22 in the primary-path maximum insertion loss, and the Zygo-STAR topology has a performance bound of 1.39 in the backup-path one. Experimental results show that our designs significantly outperform the state-of-the-art designs in wavelength usage and maximum insertion loss.

S05.3 | 14:00—14:15

Optimal Mixed-Cell-Height Detailed Placement with Spacing Cost Optimization

Da-Wei Huang, Ying-Jie Jiang, and Shao-Yun Fang
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Mixed-cell-height VLSI circuits have been popularly adopted to meet different design requirements. Due to various design for manufacturability (DFM)-related considerations, such as layout dependent effects (LDEs), drain-to-drain abutment (DDA), and pattern coloring for multiple patterning, different spacings in terms of placement sites between each pair of adjacent cells may result in different performances, which are usually modeled as discrete spacing costs. To tackle such a discrete and spacing cost-aware detailed placement problem for mixed-cell-height designs, a state-of-the-art dynamic programming (DP)-based approach can only tackle few cell rows simultaneously due to its extremely high complexity. In this paper, we propose a novel DP algorithm that can optimally and much efficiently solve the problem. In addition, several optimality-preserving reduction techniques are also proposed to enable the possibility of full-chip optimal solution derivation for large-scale designs. Experiments show that the proposed approach greatly outperforms the existing study in terms of the total spacing cost, the total displacement, and runtime.

S05.4 | 14:15—14:30

Routing Intent Aware Pin Access Point Selection for Standard Cell Designs

Po-Chun Wang, Kai-Jie Tong, and Rung-Bin Lin
Yuan Ze University

This work proposes exploiting the routing intents of a net to optimize pin access point selection. Experimental results show that our approach can significantly reduce DRC violations and achieve on average 1.4%~ 2% smaller wire length at the expense of 0.4%~2% more vias when compared with the results obtained using the access points

selected by a commercial router. Our work also performs much better than a state-of-the-art approach based on dynamic programming.

S05.5 | 14:30—14:45

DOC: A Novel DOuble Contour Based Macro Placer for Mixed-Size Designs

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Due to the rapid increase in the complexity of chip design, a chip often contains thousands of macros and millions of standard cells. In the back-end physical design, the macro placement is quite challenging nowadays. In order to quickly design low-power, high-efficiency, and low-cost chips, design factors such as the total wirelength is usually considered as an important matric. As a result, conventionally, the position of the macro in initial placement is roughly determined by minimizing the wirelength at prototyping stage. Then, at macro placement stage, the local of each macro are adjust to form a legal placement solution without increasing total wirelength. Then, the standard cells are placed. In this paper, we propose a complete macro placement framework to find legal placement result while minimizing total wirelength. Specifically, our method can be divided into two stages, the legal placement stage and optimization stage, respectively. In legal placement stage, a new concept called double contours is developed by providing another layer of contours for macro placement. Each macro can deserve more choice of placement, so that better legal placement could be obtained. In optimization stage, through our improved simulated annealing based (SA-based) algorithm, the result is further optimized by flipping and fine-tuned the position of macros. Experimental results show that our method can reduce the HPWL up to 12.5% compared with conventional single contour method.

S05.6 | 14:45—15:00

A Hotspot-Greedy Based Thermal Modeling Methodology for Smartphones

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This paper utilizes a hotspot-greedy scheme to achieve fast thermal analysis of smartphones at the pre-silicon stage. Moreover, we apply the superposed models to improve the accuracy and design a least-squares problem to extract the optimal thermal RC parameters. The proposed method can accurately simulate the system-level hotspot temperatures of smartphones with average runtime of 0.33 ms.