Oral S04

Digital Signal Processing ICs, Image/Visual & Multimedia Systems

Date/Time	8/2(三)　13:30-15:00
Chair(s)	黃柏蒼／國立陽明交通大學國際半導體產業學院 陳坤志／國立陽明交通大學電子研究所

S04.1 | 13:30—13:45

A Graph Augmentation for Semi-Supervised Learning on Skeleton-Based Action Recognition

Hung-Chih Huang, Po-Yung Chou, Cheng-Hung Lin
Department of Electrical Engineering, National Taiwan Normal University

In recent years, skeleton-based action recognition has become popular due to its higher data precision and resistance to environmental noise compared to RGB-based methods. However, the cost of annotating skeleton data is higher than RGB image data, leading to a shortage of labeled data in applications. In this study, we propose an efficient data augmentation method for skeleton data and combine it with semi-supervised learning strategies to confront the issue of low-labeled skeleton data in action recognition. In experiments using the low amount of labeled data in the NTU RGB+D dataset, our proposed method achieved an accuracy of 81.57%, compared to the 77.5% accuracy of the original method.

Index Terms-action recognition, graph convolution network, semi-supervised learning, data augmentation

S04.2 | 13:45—14:00

A Low-Complexity Hardware Implementation for Real-time Salient Object Detection based on Modified Random Color Distance and Focal Visual Prior

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The purpose of salient object detection is to extract the area of interest in an image, which often apply to real-time autofocus lens or image processing systems such as mobile devices and digital cameras. With the progress of CMOS sensor technology, it is

challenging for high resolution images to real-time implement a salient object detector in embedded systems. In this paper, the algorithm of a low computing complexity for real-time salient object detection based on random color distance (RCD) is presented. The proposed scheme combines algorithms of the histogram-based contrast, color Dispersion with modified RCD and focal visual prior. Then, the final saliency result map proposed is obtained by enhancing saliency value and morphological closing operation. Additionally, the proposed algorithm is implemented on Intel Altera FPGA Cyclone V (5CSEMA5F31C6N), which can support up to 1093 frame rate per second (FPS) at the 320 x 240 images from pubic dataset. The total hardware resources on the FPGA are 21732 LUTs and 21706 Registers. Via the analysis of computing complexity, the comprehensive performance of the proposed scheme is achieved above average. The implemented hardware on FPGA can accelerate 6 times faster than software.

S04.3 | 14:00—14:15

FPGA-Based 2D Tensor Compressive Sensing Processor for 64x64 Terehertz Single-Pixel Imaging

Yu-Heng Du, Bing-Feng Wu and Yuan-Hao Huang
Department of Electrical Engineering and Institute of Communications Engineering, National Tsing Hua University

Terahertz imaging has recently widely studied for various applications, such as defect detection of circuit and material identification for security. Single-pixel compressive sensing imaging system is one potential solution for realizing low-cost Terahertz source and detection devices in practical systems. This study aims to design a compressive sensing signal reconstruction processor for a 64x64 Terahertz single-pixel imaging system. This processor, which was implemented in a Xilinx Zynq UltraScale FPGA plate-form, achieved the best normalized throughput of 482 frame/sec and promising hardware efficiency when compared to other similar works in the literature.

S04.4 | 14:15—14:30

A Flexible and Efficient Hardware Accelerator Architecture Design for Multiple CNN

Wei-Xuan Luo, Chung-Bin Wu, Yen-Ren Hou
National Chung-Hsing University

This paper presents a novel design for a neural network accelerator that supports multiple networks and incorporates various convolution operations, including Dilated convolution and Transposed convolution. To address the SRAM data read conflicts caused by the systolic execution of convolution operations, a Forwarding mechanism is

introduced to mitigate these conflicts, and its effectiveness is demonstrated through the implementation of the Enet and Unet network. This work is of significant importance in improving the computational capabilities and expanding the application range of neural network accelerators.

S04.5 | 14:30—14:45

Separation of Time-Domain Mixtures with Different Relative Time-Delays in the ZigBee Wireless Application by Relative-Gradient Sparse Bounded-Component-Analysis Approach

Zhi-Yu Zhong, Yu-Min Wang, Er-Li Huang, and Chuen-Yau Chen
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In this paper, we apply the relative-gradient bound-component-analysis (RGBCA) algorithm in blind signal processing to separate the blind signals mixed from 16 channels which are mixed with random time-delayed image signals. In the application of ZigBee, the transmitter is a MIMO-array antennas, and the antenna elements at the receiver will receive the images arriving at different time. By modifying the number of iterations and the iteration intervals, the simulation results show that the images mixed from the original images with time difference can be separated successfully by the modified RGBCA algorithm. The simulation and verification results demonstrate this work performs well.

S04.6 | 14:45—15:00

FPGA-Based Control System for Real-Time Driving of UHD Micro-LED Display with Color Calibration

Tsung-Han Tsai, Shang-Wei Lin
Department of Electrical Engineering, National Central University

Micro-LED technology offers numerous advantages, including high brightness, low power consumption, and superior color performance. However, driving micro LED displays requires complex control algorithms and high-speed data processing. FPGA technology provides the flexibility, parallel processing capabilities, and real-time control necessary for efficient micro-LED display operation. In This work, we present the development of a real-time FPGA-based control system for a 68-inch 4K/60Hz micro-LED display. The objective of this project was to create a high-performance control system capable of driving the micro-LED display and achieving precise color accuracy. Additionally, the system was designed to support color calibration and hot plug functionality.