Oral S02

Buck Power Converters

Date/Time	8/2(三)　13:30-15:00
Chair(s)	陳柏宏／國立陽明交通大學電機工程學系 陳厚銘／國立虎尾科技大學電機工程學系

S02.1 | 13:30—13:45

A 2nd-Order Delta-Sigma-Modulation Buck Converter with Dynamic-Compensation-Controlled Techniques

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This paper presents a 2nd-order delta-sigma-modulation buck converter with dynamic-compensation-controlled (DCC) techniques. The converter's dynamic compensation control circuit consists of a current sensing circuit and a dynamic slope compensation circuit, which significantly improves the transient response. Additionally, the converter has low output noise and a fast-transient recovery time, and exhibits good undershoot and overshoot voltage control ability when the load current changes. Experimental results indicate that the buck converter is fabricated using the TSMC 0.18μm 1P6M CMOS process with a chip area of 1.13mm × 0.89mm. The sampling frequency of 10MHz, and the output-to-noise ratio (ONR) is 75.605dB. Furthermore, the converter achieves a peak power efficiency of 91.2%, with optimal performance achieved at a load current of 200 mA and an output voltage of 2.5 V.

S02.2 | 13:45—14:00

A Pseudo DCR Hysteresis Accelerated 2nd Order Delta-Sigma Modulation Buck Converter With Low-EMI

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This paper presented fast transient response and low noise buck converter with continuous-time delta-sigma-modulation (CT-DSM) technique, this technology used oversampling to give a two-stage integral loop system that can effectively move noise to high frequencies for filtering, In addition, the circuit used the pseudo DCR current sensing circuit and added the hysteresis accelerated circuit (HAC) to achieve the

function of transient acceleration. The proposed buck converter was fabricated in TSMC 0.18μm 1P6M CMOS process and the chip area is 1.12mm × 1.04mm. The measurement results show that the transient recovery time is 2.4us, 2.97us, and the undershoot, overshoot voltage is 29mV, 37mV, when the load current changes from 50mA to 500mA and from 500mA to 50mA. The output spectrum with Output to noise ratio is 71.4dB was obtained across all sampling frequencies. The max power efficiency is 91.6%, when the load current is 400mA and output voltage is 2V.

S02.3 | 14:00—14:15

A Time-Cascaded Current-Mode Buck Converter with Improved Load Regulation and Fast Transient Techniques

Mao-Ling Chiu and Tsung-Hsien Lin
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This paper presents a 2.5MHz time-cascaded current-mode buck converter with improved load regulation and fast transient techniques in CCM/DCM. The compensation of this architecture is achieved by cascading the infinite phase shift delay line (IPSDL) and VCO. The proposed compensation scheme separates the two feedback paths in the controller, optimizing the load regulation. Moreover, compared with a conventional voltage-controlled delay line, the IPSDL can cover a wide delay range while maintaining linear operation and incorporating inherent cycle-slip techniques. This allows the converter to support a wide frequency range and exhibit better transient performance. The chip is fabricated in the TSMC 180nm CMOS process. With a 3.3V input, the converter can support VOUT ranging from 0.35V to 2.6V. The load regulation is 5.26 mV/A, and the load-transient settling time is 1.4μs in CCM. The DCM is implemented to improve light-load efficiency. At 1.8V VOUT, the measured peak efficiency is 95.7%.

S02.4 | 14:15—14:30

A Dead-Beat-Controlled Buck Converter with New Current-Sensing Techniques

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This manuscript introduces a buck converter that employs advanced new current-sensing techniques, which allow for an extended input voltage range and enhanced efficiency without requiring voltage divider resistors. The circuit features dead-beat control and dynamic slope compensation, which facilitate a broad output voltage range spanning from 1 to 2.5V, and remarkably fast transient response within 0.5μs. The

proposed design was implemented using TSMC 0.18μm CMOS 1P6M technology and has a peak power efficiency of 88.3% under 350 mA load current, delivering a maximum output current of 700 mA. Furthermore, the chip has a compact footprint of 1.2 mm x 1.2 mm, including PADs.

S02.5 | 14:30—14:45

A Fixed-Switching-Frequency Quasi V2 Hysteresis-Controlled Buck Converter with New Current-Sensing and PLL-Based Techniques

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Recently, with the flourishing development of various application aspects such as IoT, AI, 5G communication. Both wearable devices and electronic communication equipment rely on stable and reliable power management chips to perform power control and management effectively, plays a very important role in these products.so this paper propose a fixed switching frequency Rippled base hysteresis Control buck converter with new active current-sensing and phase-frequency-locked techniques. The proposed converter achieves a fast dynamic transient response and high switching frequency. Under light load condition, the buck converter operate in PFM mode which reduce switching losses and improves efficiency. Propose to improve the flexibility of traditional DCR current sensing designs and effectively reduce chip area. The converter uses a phase-locked loop to maintain a fixed high switching frequency of 2MHz. The experimental results show that the converter operate over a wide load range 0.05A~ 0.7A, with an input voltage range of 3 to 4 V and an output voltage range 0.5 to 2.5 V. The fast transient response time is approximately 2 μs. The buck converter will be fabricated in TSMC 0.18μm CMOS 1P6M process. The total area of the chip is 1.2 mm x 1.2 mm. The max power efficiency is 92.05%.

Keyword: Hysteresis-Controlled, Buck Converter, Phase-Frequency-Locked (PLL) , Pulse Frequency Modulation

S02.6 | 14:45—15:00

A New Current-Sensing Hysteretic-Accelerated Second-Order Delta-Sigma Buck Converter

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A new current-sensing hysteretic-accelerated second-order delta-sigma buck converter is the circuit that uses a second-order delta-sigma modulation with oversampling and noise shaping techniques to generate a variable switching frequency to break up the output noise and achieve low electromagnetic interference. However, the transient response is relatively slow. The hysteresis -voltage-controller (HVC) circuit then generates an upper and lower voltage VBH and VBL. If the voltage VSen is less than the lower voltage VBL or the voltage VSen is greater than the upper voltage VBH, the power transistors MN and MP are switched on to achieve transient response acceleration. The transient times are 2.8μs and 3.0μs when the load current is varied between 500mA and 50mA, respectively, and the peak conversion efficiency is 87.8% at an output voltage of 2.5V with a load current of 250mA.