Oral S01

Analog Circuits and Sensor Interfaces

Date/Time	8/2(三) 13:30-15:00
Chair(s)	林群祐／國立臺灣師範大學電機工程學系 劉仁傑／國立聯合大學電機工程學系

S01.1 | 13:30—13:45

A Current Adaptation Buffer Amplifier with Transient Improvement

Zu-Jia Lo, Yun-Jie Huang, Ren-Yong Hung, Tzu-Heng Hsu, Hsiu-Min Yang, Xiu-Zhu Li, Yuan-Chuan Wang, Yung-Chi Cheng, Sheng-Yu Peng
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This paper proposes a transient enhanced autonomous current adaptation buffer amplifier (ACABA) that effectively resolves the slew rate degradation problem observed in the previous design. The proposed circuit enhances the transient responses, achieving faster step responses, superior linearity, and higher power efficiency. The cause of the degradation in the previous work has been elucidated, and a transient enhancement circuit is proposed to circumvent the slewing bottleneck. A prototype chip has been designed and fabricated in a 0.35 μm CMOS process. From measurements, the proposed circuit improves settling time by 62.1%, enhances slew rate by 3.1 times, and reduces total harmonic distortion (THD) by 17 dB without extra static power consumption. With a 2.5V supply voltage, the proposed buffer amplifier allows a maximum input signal amplitude of 2.3 V with the THD below −60 dB. Furthermore, the enhanced buffer amplifier exhibits the best power efficiency in both small-signal and large-signal performance compared to other state-of-the-art designs

S01.2 | 13:45—14:00

The Integration of Ladder-Based DACs with 6T-SRAMs for Cognitive Computation in Edge Applications

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A reconfigurable cognitive computation matrix (RCCM) in static random access memory

(SRAM) suitable for sensor edge applications is proposed in this paper. The proposed RCCM can take multiple analog currents or digital integers as the input vector and performs vector-matrix multiplication with a weight integer matrix. The RCCM can carry out 1-quadrant, 2-quadrant, or 4-quadrant multiplications in the analog domain. Therefore, the digital integers for the inputs or weights stored in the SRAM can be either signed or unsigned, providing extensive usage flexibilities. Furthermore, three commonly used activation functions, the rectified linear unit (ReLU), radial basis function (RBF), and logistic function, are available, converting multiply accumulation outputs to single-ended currents as the computation results. The resultant output currents can be adopted as the input currents of other RCCMs to facilitate multiple-layer network implementation. A concept-proving prototype chip, including a 16 × 16 RCCM with 4-bit input and weight resolutions, is designed and fabricated in a 0.18 μm CMOS process. The computation accuracy that is deteriorated by process variation can be significantly improved by adopting 64 mismatch parameters after calibration. A handwritten digit recognition database, MNIST, is employed to evaluate the chip performance, achieving average efficiency of 3.355TOPS/W.

S01.3 | 14:00—14:15

An 18 nW, 170 °C Temperature Range, Voltage, and Current Reference Circuit with Low Line Sensitivity

I-Fan Lin, Yu-Chu Tsai, Heng-Li Lin, and Yu-Te Liao
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Abstract—This paper presents a hybrid voltage and current reference (VCR) design in a 0.18-μm CMOS process. The cascode current mirror and stacked-diode MOS-transistors (SDMTs) of the voltage reference (VR) provide stable voltage and current insensitive to the supply. The SDMT creates a voltage complementary to absolute temperature (CTAT) for the current reference (CR) bias. Moreover, the CTAT voltage corresponds to the temperature coefficient (TC) of the resistor. A pseudo resistor is added in the VR, and a VREF-biased NMOS is added in the CR for temperature compensation. This design achieves a TC of 123 ppm/°C in VR and 266 ppm/°C in CR from the temperature range of -40 °C °C to 130 °C. A line sensitivity (LS) of 0.011%/V and 0.094%/V is attained in VR and CR, respectively, while only consuming 18.51 nW. The active area of the VCR is 25000 μm2.

S01.4 | 14:15—14:30

A CMOS Buffer Amplifier with Slew-Rate Enhancement for Display applications

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This paper presents a low-power buffer amplifier with a high slew rate. The buffer amplifier with cross-coupled input pairs and positive feedback enhances the driving current at the transients dynamically. The adaptive bias-switching scheme reduces static power consumption. The design was fabricated in a 0.18-μm CMOS process. The proposed amplifier offers a slew rate of 13.42 V/μs at a load capacitor of 100 pF with a static current of 2.38 μA, which is 80 times better than the one without the current-boosting scheme. The chip area is 189 x 144 μm2.

S01.5 | 14:30—14:45

Characterization of ESD-Induced Electromigration on Metal Lines in On-Chip ESD Protection Circuit

Yang-Shou Hou and Chun-Yu Lin
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Electrostatic discharge (ESD) events are a significant reliability issue for ICs, and designing on-chip ESD protection is crucial. However, research on metal lines during ESD events is limited. This paper analyzes ESD-induced electromigration (EM) of metal lines, identifies metal sensitivity to component-level ESD events in the CMOS process, and estimates ESD robustness. The study results can help inform the design of metal lines for ESD protection in ICs.

S01.6 | 14:45—15:00

ESD Protection Circuit Design for Multiple Power Domains

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Integrated circuits, which are becoming increasingly complex, usually incorporate more circuits and generally include at least two power domains. Given that ESD events can occur between any two power supplies, it is important to design each discharge path to release ESD current effectively. In this work, a new ESD protection design called NMOS-Triggered Dual-Power Silicon-Controlled Rectifier (NMT_DP_SCR) is proposed. The protection design integrates twelve discharge paths required for a dual-power-domain IC and reduces the trigger voltage of the device by using two grounded features of the dual power supply. The protection device is demonstrated in a 0.18μm CMOS process. The proposed design can effectively reduce the area required for ESD protection and provide better ESD protection for dual power supply circuits.